

QDD-2X100G-CWDM4

2x100GBASE-CWDM4 QSFP28-DD, SMF, 1270nm-1330nm, 2km, 2xCS, DOM

Features

- Supports 206Gbps
- Single 3.3V Power Supply
- Power dissipation < 8.0W
- Up to 2km over SMF
- QSFP-DD MSA Compliant
- 8x25G electrical interface
- Dual CS connector
- Commercial case temperature range of 0°C to 70°C
- 8*25Gbps DFB-based CWDM transmitter
- PIN and TIA array on the receiver side
- I²C interface with integrated Digital Diagnostic Monitoring
- Safety Certification: TUV/UL/FDA
- RoHS compliant

Applications

- 2x100G QSFP-DD CWDM4 applications with FEC

Description

Fibrenet' QSFP-DD transceiver module is designed for use in 200 Gigabit Ethernet links over 2km single mode fiber. The implementation of an 8 channel TOSA and ROSA to create a Dual CWDM4 transceiver. The 8 channel optical engines, which include dual embedded CWDM4 multiplexers. The 2x100G CWDM4 QSFP-DD transceiver is characterized by an 8x25G NRZ electrical interface and Dual CS connectors and compliant with QSFP-DD MSA.

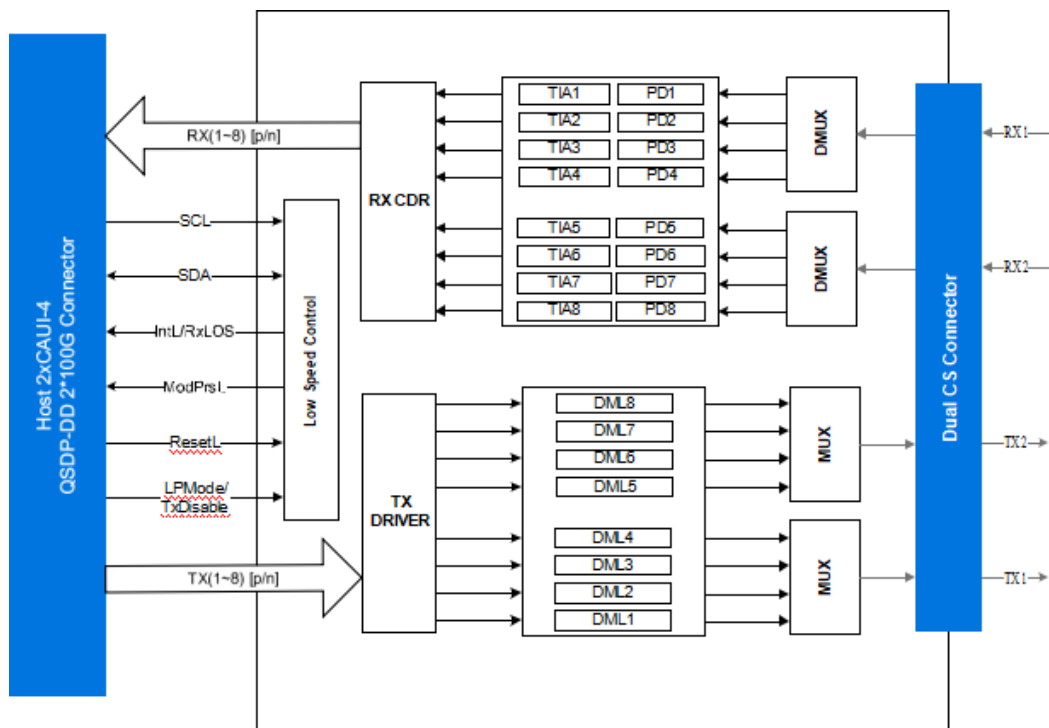


Figure 1: Transceiver Block Diagram

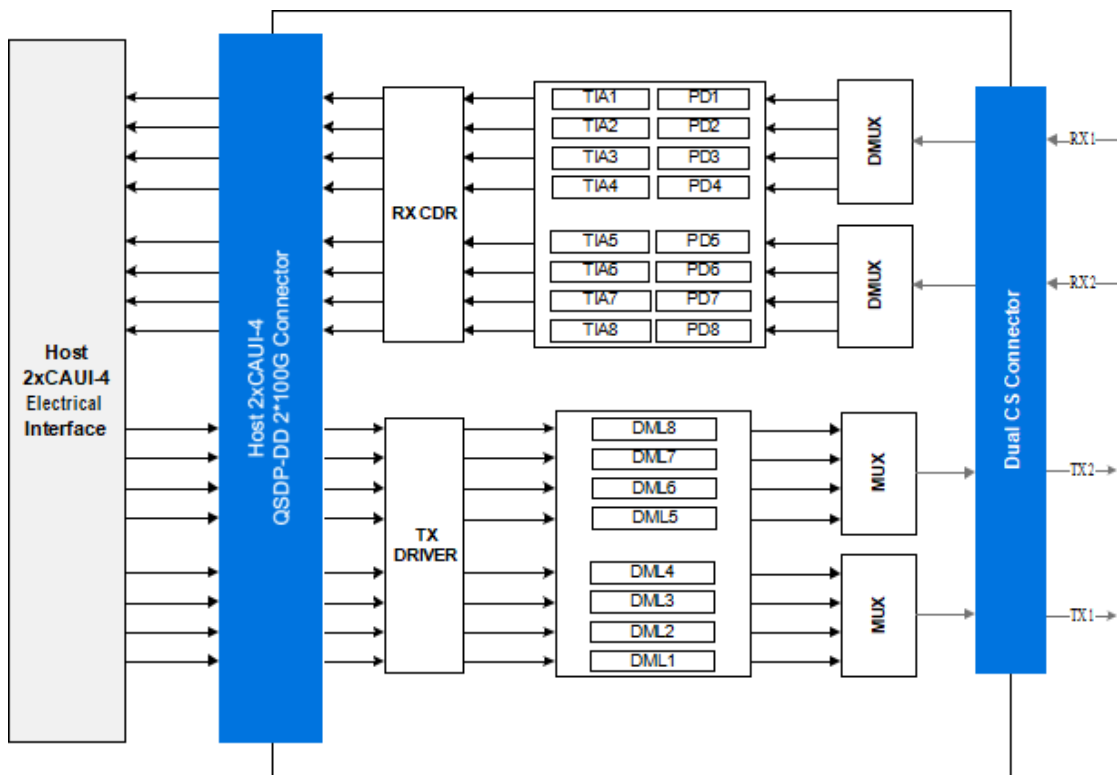


Figure 2: Application Reference Diagram

Transmitter

As shown in Figure 1, the transmitter path of the transceiver contains an 8x25Gbps 2xCAUI-4 electrical input with Equalization (EQ) block, optical multiplexer, DML laser driver, diagnostic monitors and 8 directly modulated laser.

Receiver

As shown in Figure 1, the receiver path of the transceiver contains eight PIN photodiodes, trans-impedance amplifiers (TIA), de-multiplexer and 8x25G 2xCAUI-4 compliant electrical output blocks. The Rx Output Buffer provides CAUI-4 compliant differential outputs for the high speed electrical interface.

High Speed Electrical Signal Interface

The interface between QSFP-DD module and ASIC/SerDes is shown in Figure 2. The high speed signal lines are internally DC-coupled and the electrical inputs are internally terminated to 100 Ohms differential. All transmitter and receiver electrical channels are compliant to module CAUI-4 specifications per IEEE 802.3bm.

Control Signal Interface

The control signal interface is compliant with QSFP-DD MSA. The following pin is provided to control module or display the module status: ModSelL, ResetL, LPMode/TxDisable, ModePrsL, IntL/RxLOSL. In addition, there is an industry standard two wire serial interface scaled for 3.3V LVTTTL. The definition of control signal interface and the registers of the serial interface memory are defined in the Control Interface & Memory Map section.

Handling and Cleaning

Exposure to current surges and overvoltage events can cause immediate damage to the transceiver module. Observe the precautions for normal operation of electrostatic discharge sensitive equipment; Attention shall also be paid to limiting transceiver module exposure to conditions beyond those specified in the absolute maximum ratings.

Optical connectors include female connectors. These elements will be exposed as long as the cable or port plug is not inserted. At this time, always pay attention to protection.

Each module is equipped with a port guard plug to protect the optical port. The protective plug shall always be in place whenever the optical fiber is not inserted. Before inserting the optical fiber, it is recommended to

clean the end of the optical fiber connector to avoid contamination of the module optical port due to dirty connector. If contamination occurs, use standard CS port cleaning methods.

Absolute Maximum Ratings*4

Exceeding the absolute maximum ratings table may cause permanent damage to the device. This is just an emphasized rating, and does not involve the functional operation of the device that exceeds the specifications of this technical specification under these or other conditions. Long-term operation under absolute maximum ratings will affect the reliability of the device.

Parameter	Symbol	Min	Typical	Max	Unit
Storage Temperature	Ts	-40		+85	°C
3.3 V Power Supply Voltage	Vcc	-0.5	3.3	3.6	V
Data Input Voltage – Single Ended		-0.5		Vcc+0.5	V
Data Input Voltage – Differential*5				0.8	V
Operating Relative Humidity	RH	5		85	%
Receiver Damage Threshold, per Lane	Rxdmg	3.5			dBm

*4: Exceeding any one of these values may damage the device permanently.

*5: This is the maximum voltage that can be applied across the differential inputs without damaging the input circuitry. The damage threshold of the module input shall be at least 1600 mV peak to peak differential.

Recommended Operating Conditions*6

For operations beyond the recommended operating conditions, optical and electrical characteristics are not defined, reliability is not implied, and such operations for a long time may damage the module.

Parameter	Symbol	Min	Typical	Max	Unit
Operating case temperature*7	Tc	0	25	70	°C
Power supply voltage	Vcc	3.135	3.3	3.465	V
Power dissipation	PD			8	W
Electrical Signal Rate per Channel*8			25.78125		GBd
Optical Signal Rate per Channel*9			25.78125		GBd
Power Supply Noise*10				66	mVpp
Receiver Differential Data Output Load		100			Ohm

*6: Power Supply specifications, Instantaneous, sustained and steady state current compliant with QSFP-DD MSA Power Classification.

*7: The position of case temperature measurement is shown in Figure 9. Continuous operation at the maximum Recommended Operating Case Temperature should be avoided in order not to degrade reliability.

*8: CAUI-4 operation with Host generated FEC. The transmitter must receive pre-coded FEC signals from the host ASIC.

*9: 2x100G FR4 operation with Host generated FEC. The transmitter must receive pre-coded FEC signals from the host ASIC.

*10: Power Supply Noise is defined as the peak-to-peak noise amplitude over the frequency range at the host supply side of the recommended power supply filter with the module and recommended filter in place. Voltage levels including peak-to-peak noise are limited to the recommended operating range of the associated power supply. See Figure 7 for recommended power supply filter.

General Electrical Characteristics*11

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Parameter	Symbol	Min	Typical	Max	Unit
Transceiver Power Consumption				8	W
Transceiver Power Supply Current, Total				2560	mA

Reference Points

Test Point	Description
TP0 to TP5	The channel including the transmitter and receiver differential controlled impedance printed circuit board insertion loss and the cable assembly insertion loss.
TP1 to TP4	All cable assembly measurements are to be made between TP1 and TP4 as illustrated in Figure 3. The cable assembly test fixture of Figure 4 or its equivalent, is required for measuring the cable assembly specifications in 802.3bj 92.10 at TP1 and TP4.
TP0 to TP2 TP3 to TP5	A mated connector pair has been included in both the transmitter and receiver specifications defined in 802.3bj 92.8.3 and 92.8.4. The recommended maximum insertion loss from TP0 to TP2 or from TP3 to TP5 including the test fixture is provided in 802.3bj 92.8.3.6
TP2	Unless specified otherwise, all transmitter measurements defined in 802.3bj 92.6 are made at TP2 utilizing the test fixture specified in 802.3bj 92.11.1.
TP3	Unless specified otherwise, all receiver measurements and tests defined in 802.3bj 92.8.4 are made at TP3 utilizing the test fixture specified in 802.3bj 92.11.1.

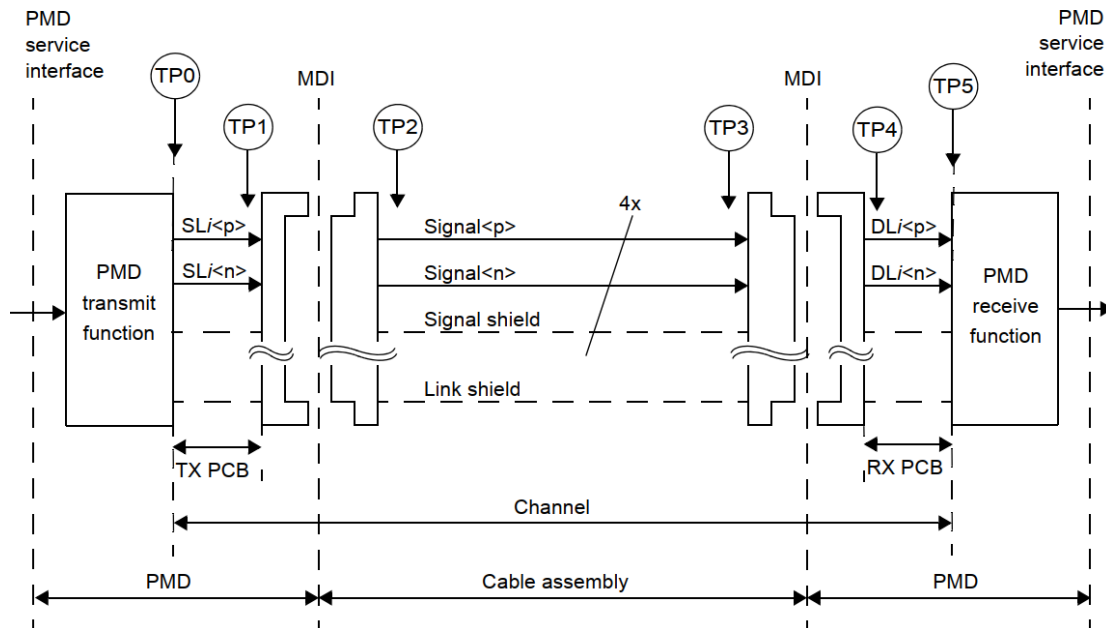


Figure 3: IEEE 802.3bj 100GBASE-CR4 link

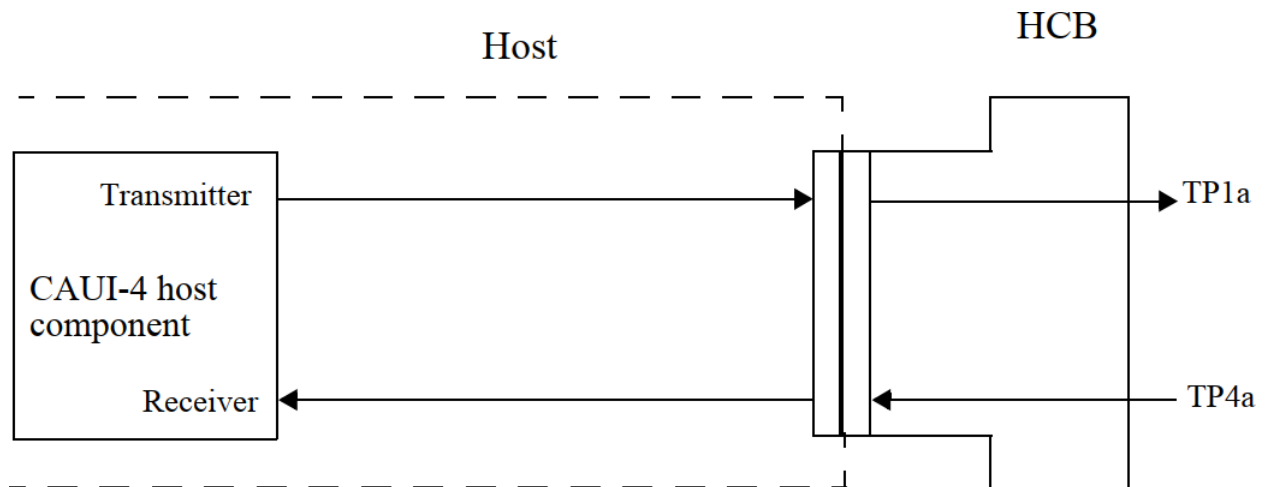


Figure 4: IEEE 802.3bm CAUI-4 compliance points TP1a, TP4a

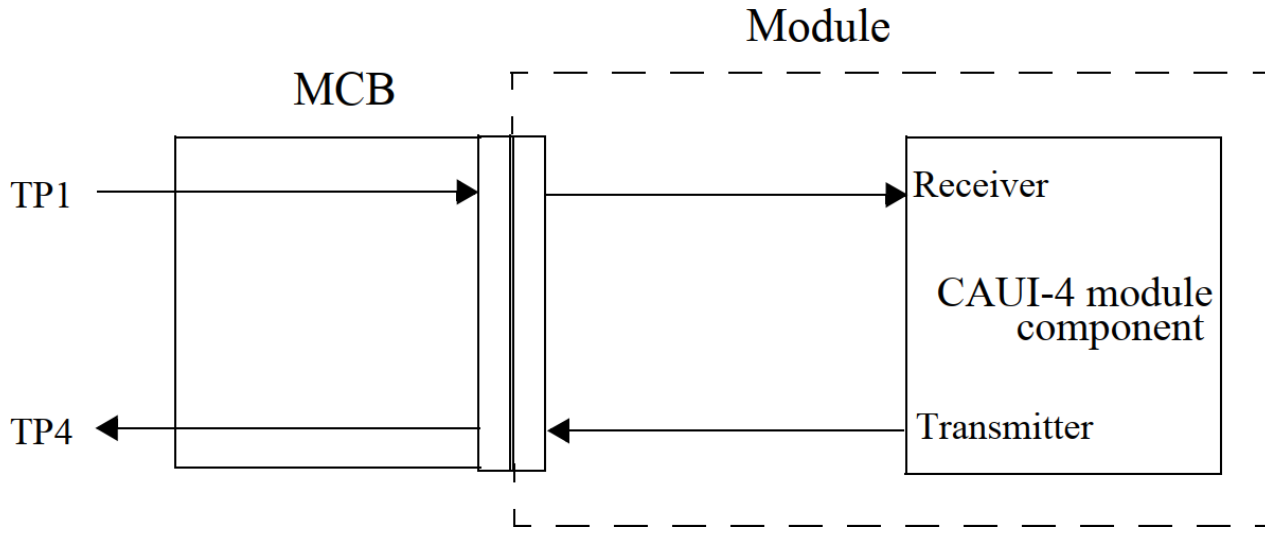


Figure 5: IEEE 802.3bm CAUI-4 compliance points TP1, TP4

High Speed Electrical Input Characteristics

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Parameter	Test Point	Min.	Typical	Max.	Unit	Conditions
Signaling Rate, Per Lane	TP1		25.78125		GBd	+/- 100 ppm
Differential pk-pk Input Voltage Tolerance	TP1a	900			mV	
Differential Return Loss(min)	TP1	Equation(83E-5)			dB	802.3bm
Differential to common mode input return loss (min)	TP1	Equation(83E-6)			dB	802.3bm
Differential termination mismatch	TP1			10	%	
Module stressed input test	TP1a					
Single-ended voltage tolerance range	TP1a	-0.4		3.3	V	
DC common-mode output voltage*12	TP1	-350		2850	mV	
Module stressed input test *13						
Eye width			0.46		UI	
Applied pk-pk sinusoidal jitter			Table 88-13			802.3bm
Eye height			95		mV	

*12: DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

*13: Module stressed input tolerance is measured using the procedure defined in 83E.3.4.1.1.

High Speed Electrical Output Characteristics

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Parameter	Test Point	Min.	Typical	Max.	Unit
Signaling Rate, Per Lane(range)	TP4		25.78125 ± 100 ppm		GBd
Differential output voltage	TP4			900	mV
Differential output return loss (Min)	TP4	Equation (83E-2)			dB
Common to differential mode conversion return loss (min)	TP4	Equation (83E-3)			dB
Differential termination mismatch	TP4			10	%
DC common mode voltage	TP4	-0.35		2.85	V
Transition Time (20% to 80%)	TP4	12			ps
Eye width	TP4	0.57			UI
Eye height differential	TP4	228			mV
Vertical eye closure	TP4			5.5	dB

High Speed Optical Transmitter Characteristics

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Optical Characteristics @TP2 Test Point

Parameter	Symbol	Min.	Typical	Max.	Unit
Signaling speed per lane	BRAVE		25.78125		Gbps
Data Rate Variation		-100		+100	ppm
Modulation format		NRZ		1317.5	nm
Lane_0/4 Center Wavelength	λ_{C0}	1264.5		1277.5	nm
Lane_1/5 Center Wavelength	λ_{C1}	1284.5		1297.5	nm
Lane_2/6 Center Wavelength	λ_{C2}	1304.5		1317.5	nm
Lane_3/7 Center Wavelength	λ_{C3}	1324.5		1337.5	nm
Total Average Output Power	Po			8.5	dBm
Side Mode Suppression Ratio	SMSR	30			dB
Extinction Ratio	ER	3.5			dB
Average Launch Power each Lane*14	Peach	-6.5		2.5	dBm
Transmit OMA each Lane *15	TxOMA	-4.0		2.5	dBm
Launch power in OMA minus TDP, each lane	OMA-TDP	-5.0			dBm
Transmitter and Dispersion Penalty per Lane *16	TDP			3	dB

Average launch power of OFF transmitter				-30	dBm
Optical Return Loss Tolerance				20	dB
Transmitter Reflectance *17				-12	dB
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}*18		{0.31, 0.4, 0.45, 0.34, 0.38, 0.4}			

*14: Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.

*15: Even if the TDP < 1.0dB, the OMA (min) must exceed this value.

*16: TDP does not include a penalty for multi-path interference (MPI).

*17: Transmitter reflectance is defined looking into the transmitter.

*18: Hit ratio of 5×10^{-5}

High Speed Optical Receiver Characteristics

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Optical Characteristics @TP3 Test Point

Parameter	Symbol	Min.	Typical	Max.	Unit
Signaling Speed per Lane	BRAVE		25.78125		Gbps
Data Rate Variation		-100		+100	ppm
Lane_0/4 Center Wavelength	λ_{C0}	1264.5		1277.5	nm
Lane_1/5 Center Wavelength	λ_{C1}	1284.5		1297.5	nm
Lane_2/6 Center Wavelength	λ_{C2}	1304.5		1317.5	nm
Lane_3/7 Center Wavelength	λ_{C3}	1324.5		1337.5	nm
Damage threshold	Rxdmg	3.5			dBm
Average receive power each lane*19	Rxpow	-11.5		2.5	dBm
Receive Power (OMA) per Lane	RxOMA			2.5	dBm
Unstressed Receiver Sensitivity (OMA) per Lane *20	Rxsens			-10	dBm
Stressed Receiver Sensitivity (OMA) per Lane *21	RXSRS			-7.3	dBm
Vertical Eye Closure Penalty *22	VECP	1.9			dB
Stressed J2 Jitter *22	J2	0.33			UI
Stressed J4 Jitter *22	J4	0.48			UI
SRS eye mask definition {X1, X2, X3, Y1, Y2, Y3} *22		{0.39, 0.5, 0.5, 0.39, 0.39, 0.4}			
LOS Assert	LOSA	-25			dBm
LOS De-Assert	LOSD			-12	dBm
LOS Hysteresis		0.5			dB

RSSI accuracy		-3		+3	dB
Receiver reflectance				-26	dB

*19: Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

*20: Sensitivity is specified at 5×10^{-5} BER.

*21: Measured with conformance test signal at TP3 for BER = 5×10^{-5} .

*22: Vertical eye closure penalty, stressed eye J2 Jitter, stressed eye J4 Jitter, and SRS eye mask definition are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Regulatory Compliance Issues

Various standard and regulations apply to the QDD-2002C31-02CC modules. These include eye-safety, Component Recognition, RoHS, ESD, EMC and Immunity. Please note the transmitter module is a Class 1 laser product. See Regulatory Compliance Table for details.

Regulatory Compliance Table

Feature	Test Method	Performance
Laser Eye Safety and Equipment Type Testing 	(IEC) EN 62368-1:2014+A11 (IEC) EN 60825-1:2014 (IEC) EN 60825-2:2004+A1+A2	CDRH Accession Number:2132182-000 TUV File: R 50457725 0001 CB File: JPTUV-100513
Component Recognition	Underwriters Laboratories (UL) and Canadian Standards Association (CSA) Joint Component Recognition for Information Technology Equipment including Electrical Business Equipment	UL File: E317337
RoHS Compliance	RoHS Directive 2011/65/EU&(EU)2015/863	Less than 100 ppm of cadmium. Less than 1000 ppm lead, mercury, hexavalent chromium, poly brominated biphenyls (PPB), poly brominated biphenyl ethers (PBDE), dibutyl phthalate, butyl benzyl phthalate, bis (2-ethylhexyl) phthalate and diisobutyl phthalates.
Electrostatic Discharge (ESD) to the Electrical Contacts	JEDEC Human Body Model (HBM) (JESD22-A114-B)	High speed contacts shall withstand 1000V. All other contacts shall withstand 2000 V.

Electrostatic Discharge (ESD) to the Optical Connector Receptacle	IEC 61000-4-2:2008	When installed in a properly grounded housing and chassis the units are subjected to 15kV air discharges during operation and 8kV direct discharges to the case.
Electromagnetic Interference (EMI)	FCC Part 15 Class B; CISPR 32 (EN55032) 2015;	System margins are dependent on customer board and chassis design.
Immunity	IEC 61000-4-3:2010; EN55035:2017	Typically shows no measurable effect from a 10V/m field swept from 80 MHz to 1 GHz applied to the module without a chassis enclosure.

Electrostatic Discharge (ESD)

The QDD-2002C31-02CC is complies with the ESD requirements described in the Regulatory Compliance Table. However, in the normal processing and operation of optical transceiver, the following two types of situations need special attention.

Case I: Before inserting the transceiver into the rack meeting the requirements of QSFP-DD MSA, ESD preventive measures must be taken to protect the equipment. For example, the grounding wrist strap,workbench and floor should be used wherever the transceiver is handled.

Case II: After the transceiver is installed, the electrostatic discharge outside the chassis of the host equipment shall be within the scope of system level ESD requirements. If the optical interface of the transceiver is exposed outside the host equipment cabinet, the transceiver may be subject to equipment system level ESD requirements.

Electromagnetic Interference (EMI)

Communication equipment with optical transceivers is usually regulated by FCC in the United States and CENELEC EN55032 (CISPR 32) in Europe. The compliance of QDD-2002C31-02CC with these standards is detailed in the regulatory compliance table. The metal shell and shielding design of QDD-2002C31-02CC will help equipment designers minimize the equipment level EMI challenges they face.

Flammability

QDD-2002C31-02CC optical transceiver meets UL certification requirements, its constituent materials have heat and corrosion resistance, and the plastic parts meet UL94V-0 requirements.

QSFP-DD Transceiver Electrical Pad Layout

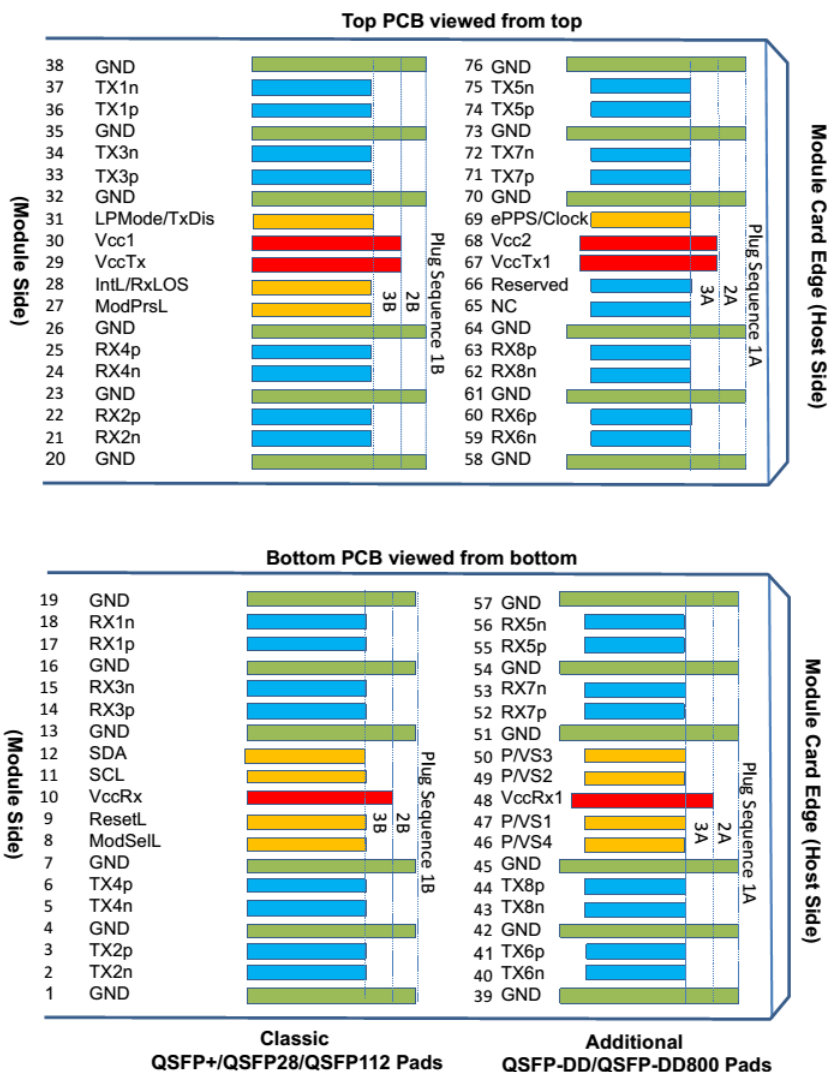


Figure 6: QSFP-DD Module Pinout

Pin Arrangement and Definition

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	

4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVC MOS- I/O	SCL	TWI serial interface clock	3B	
12	LVC MOS- I/O	SDA	TWI serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1n	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt/optional RxLOS	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	LPMoDe/ TxDis	Low Power Mode/optional TX Disable	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	

42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46	LVC MOS/CML-I	P/VS4	Programmable/Module Vendor Specific 4	3A	3
47	LVC MOS/CML-I	P/VS4	Programmable/Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49	LVC MOS/CML-O	P/VS2	Programmable/Module Vendor Specific 2	3A	3
50	LVC MOS/CML-O	P/VS3	Programmable/Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69	LVC MOS-I	ePPS/ Clock	1PPS PTP clock or reference clock input	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

1: QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFPDD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane. Each connector GND contact is rated for a maximum current of 500 mA

- 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Supply requirements defined for the host side of the Host Card Edge Connector are listed in QSFP-DD MSA. For power classes 4 and above the module differential loading of input voltage pads must not result in exceeding contact current limits. Each connector Vcc contact is rated for a maximum current of 1500 mA.
- 3: All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.
- 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.
- 5: Full definitions of the P/VSx signals currently under development. On new designs not used P/VSx signals are recommended to be terminated on the host with 10k ohms.
- 6: ePPS/Clock if not used recommended to be terminated with 50 ohms to ground on the host.

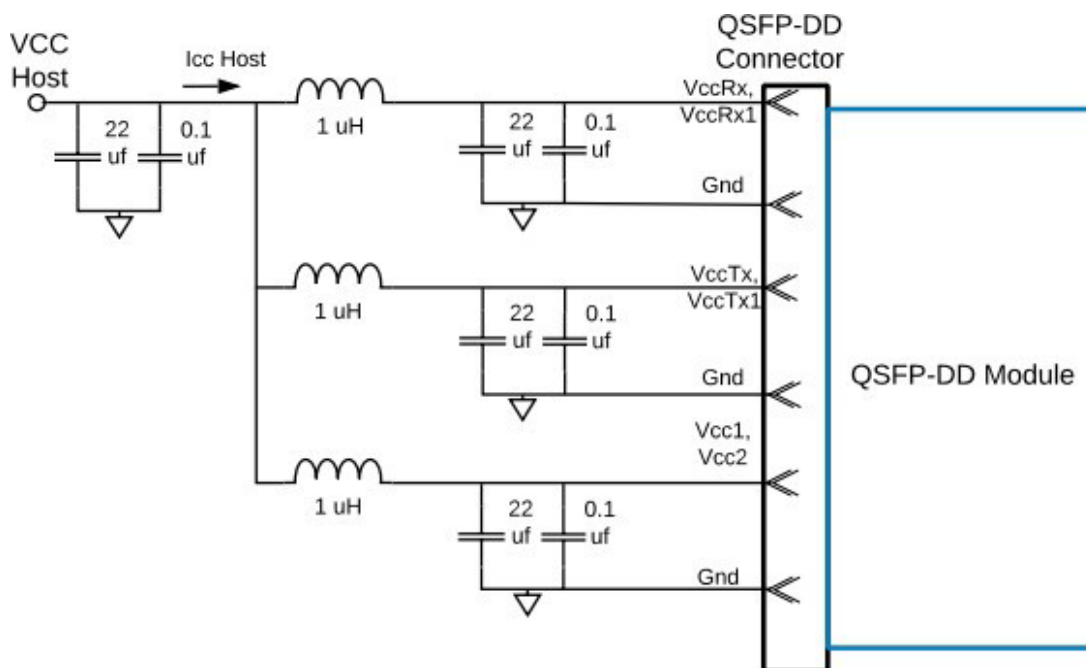


Figure 7: Host Board Power Supply Filter

During power transient events, the host should ensure that any neighboring modules sharing the same supply stay within their specified supply voltage limits. The host should also ensure that the intrinsic noise of the power rail is filtered in order to guarantee the correct operation of the optical modules.

Package Outline

The module is designed to meet the package outline defined in the QSFP-DD MSA specification. See the package outline for details.

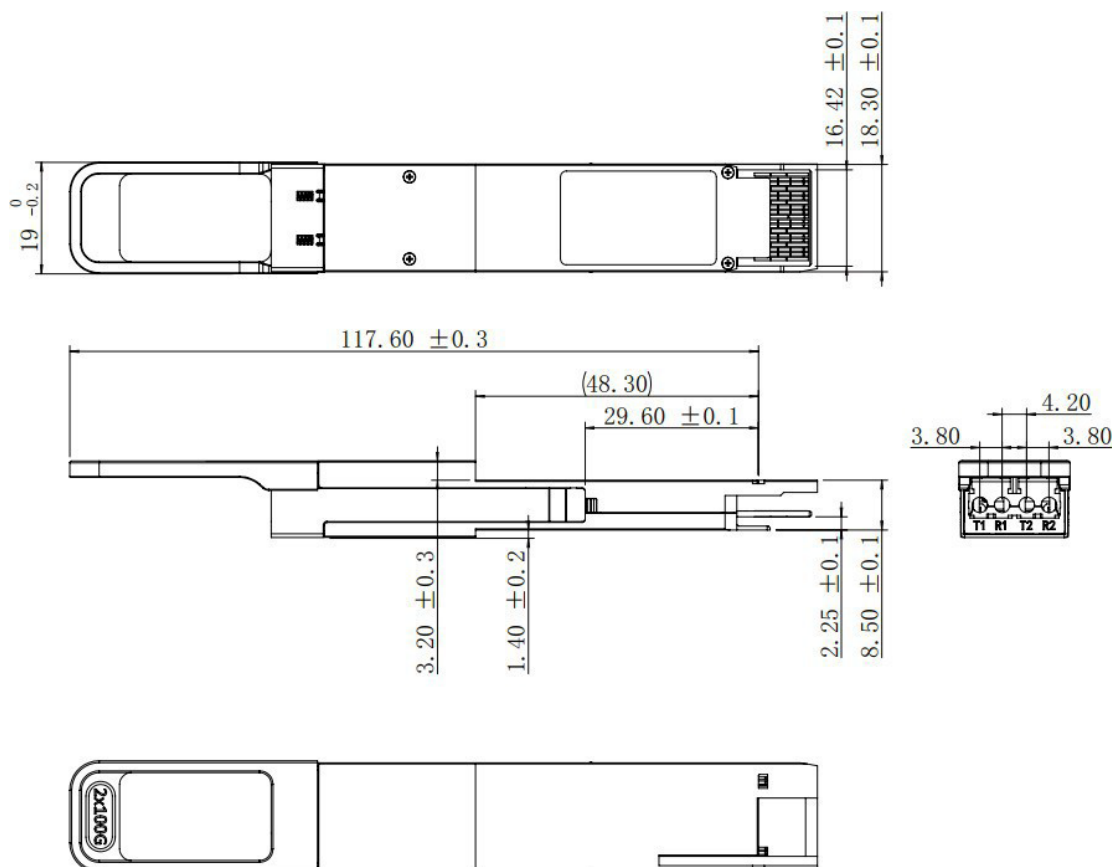


Figure 8: Mechanical Package Outline (All dimensions in mm)

The bellow picture shows the location of the hottest spot for measuring module case temperature. In addition, the digital diagnostic monitors (DDM) temperature is also calibrated to this spot.

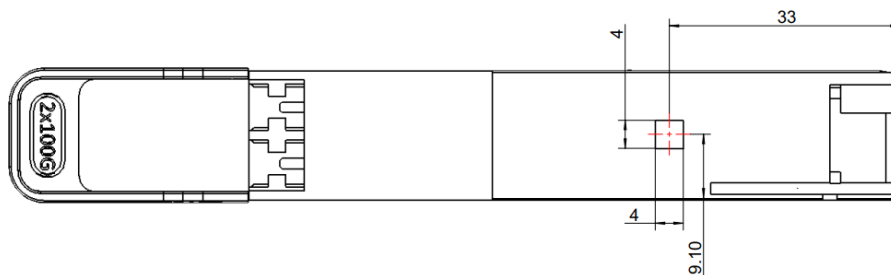


Figure 9: Case Temperature Measurement Point (All dimensions in mm)

The optical interface port is a dual CS connector as specified in CS-01242017.

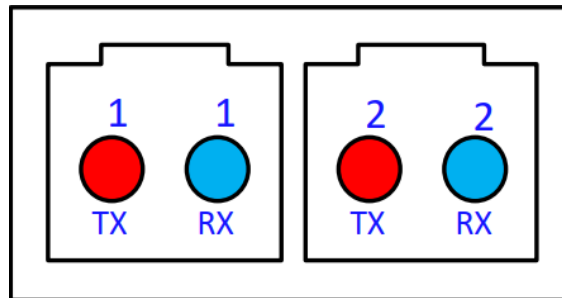


Figure 10: Module Optical Interface (looking into the optical port)

Control Interface & Memory Map

The control interface combines dedicated signal lines for ModSelL, ResetL, LPMode/TxDisable, ModPrsL, IntL/RxLOSL with two-wire serial (TWS), interface clock (SCL) and data (SDA), signals to provide users rich functionality over an efficient and easily used interface.

SCL and SDA

The SCL and SDA is a hot plug interface that may support a bus topology. During module insertion or removal, the module may implement a pre-charge circuit which prevents corrupting data transfers from other modules that are already using the bus.

ModSelL

The ModSelL is an input signal that shall be pulled to Vcc in the QSFP-DD modules. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP-DD modules on a single 2-wire interface bus. When ModSelL is “High”, the module shall not respond to or acknowledge any 2-wire interface communication from the host.

In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any QSFP-DD modules are deselected. Similarly, the host must wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

ResetL

The ResetL signal shall be pulled to Vcc in the module. A low level on the ResetL signal for longer than the minimum pulse length (10us) initiates a complete module reset, returning all user module settings to their default state.

LPMODE/TxDisable

LPMODE/TxDis is a dual-mode input signal from the host operating with active high logic. It shall be pulled towards Vcc in the module. At power-up or after ResetL is deasserted LPMODE/TxDis behaves as LPMODE. If supported, LPMODE/TxDis can be configured as TxDisable using the two-wire interface except during the execution of a reset. LPMODE is used in the control of the module power mode.

When LPMODE/TxDis is configured as LPMODE, the module behaves as though TxDisable=0. By using the LPMODE signal and a combination of the Power_override, Power_set and High_Power_Class_Enable software control bits the host controls how much power a module can consume. When LPMODE/TxDisable is configured as TxDisable, the module behaves as though LPMODE=0.

Changing LPMODE/TxDisable mode from LPMODE to TxDisable when the LPMODE/TxDisable state is high disables all optical transmitters. If the module was in low power mode, then the module transitions out of low power mode at the same time. If the module is already in high power state (Power Override control bits) with transmitters already enabled, the module shall disable all optical transmitters. Changing the LPMODE/TxDisable mode from LPMODE to TxDisable when the LPMODE/TxDisable state is low, simply changes the behavior of the mode of LPMODE/TxDisable. The behavior of the module depends on the Power Override control bits.

Note that the “soft” functions of TxDisable, LPMODE, IntL and RxLOSL allow the host to poll or set these values over the two-wire interface as an alternative to monitoring/setting signal values. Asserting either the “hard pin” or “soft bit” (or both) for TxDisable or LPMODE results in that function being asserted.

ModPrsL

ModPrsL shall be pulled up to Vcc Host on the host board and pulled low in the module. The ModPrsL is asserted “Low” when the module is inserted. The ModPrsL is deasserted “High” when the module is physically absent from the host connector due to the pull-up resistor on the host board.

IntL/RxLOSL

IntL/RxLOSL is a dual-mode active-low, open-collector output signal from the module. It shall be pulled up towards Vcc on the host board. At power-up or after ResetL is released to high, IntL/RxLOSL is configured as IntL. When the IntL signal is asserted Low it indicates a change in module state, a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL signal is deasserted “High” after all set interrupt flags are read. If dual mode operation supported, IntL/RxLOSL can be optionally programmed as RxLOSL using the two-wire interface except during the execution of a reset. If the module has no interrupt flags asserted (IntL/RxLOSL is high), there should be no change in IntL/RxLOSL states after the mode change.

If IntL/RxLOSL is configured as RxLOSL, a low indicates that there is a loss of received optical power on at least one lane. “High” indicates that there is no loss of received optical power. The actual condition of loss of optical receive power is specified by other governing documents, as the alarm threshold level is application specific. The module shall pull RxLOSL to low if any lane in a multiple lane module or cable has a LOS condition and shall release RxLOSL to high only if no lane has a LOS condition.

Low Speed Control and Sense Signals

Parameter	Symbol	Min.	Typical	Max.	Unit
SCL and SDA	VOL	0		0.4	V
SCL and SDA	VIL	-0.3		VCC*0.3	V
	VIH	VCC*0.7		VCC+0.5	V
Capacitance for SCL and SDA I/O signal	Ci			14	pF
Total bus capacitive load for SCL and SDA	Cb			100	pF
				200	pF
LPMode/TxDisable, ResetL, ModSelL and ePPS/Clock	VIL	-0.3		0.8	V
	VIH	2		VCC+0.3	V
LPMode, ResetL and ModSelL	lin			360	μA
IntL/RxLOSL	VOL	0		0.4	V
	VOH	VCC-0.5		VCC+0.3	V
ModPrsL	VOL	0		0.4	V
	VOH				

Memory Map

The control interface and memory map of the QSFP-DD module is compliant with the QSFP-DD MSA. The QSFP-DD module support I2C interface protocol defined by the QSFP-DD MSA. Access clock frequency support a minimum of 100 kHz with no clock stretching and burst read/write of at least 32 bytes.

The module meets the following requirements:

1. The module initialize in hardware mode when LPMode is de-asserted.
2. The transmitter is disabled when the module is held in reset.
3. Tx Squelch function is implemented as defined by the QSFP-DD MSA. When squelched, the transmitter remains on with the modulation turned off.
4. Rx Squelch function is implemented as defined by the QSFP-DD MSA. When Rx CDR LOS is asserted, CDR output is squelched.

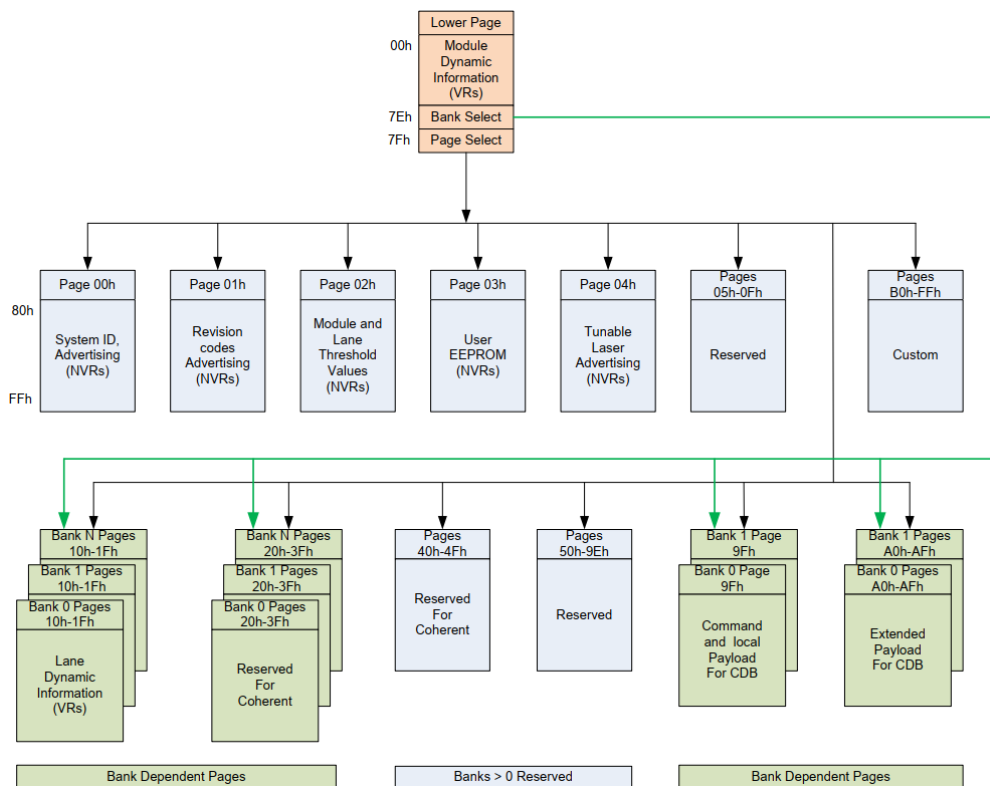


Figure 11: QSFP-DD CMIS Module Memory Map

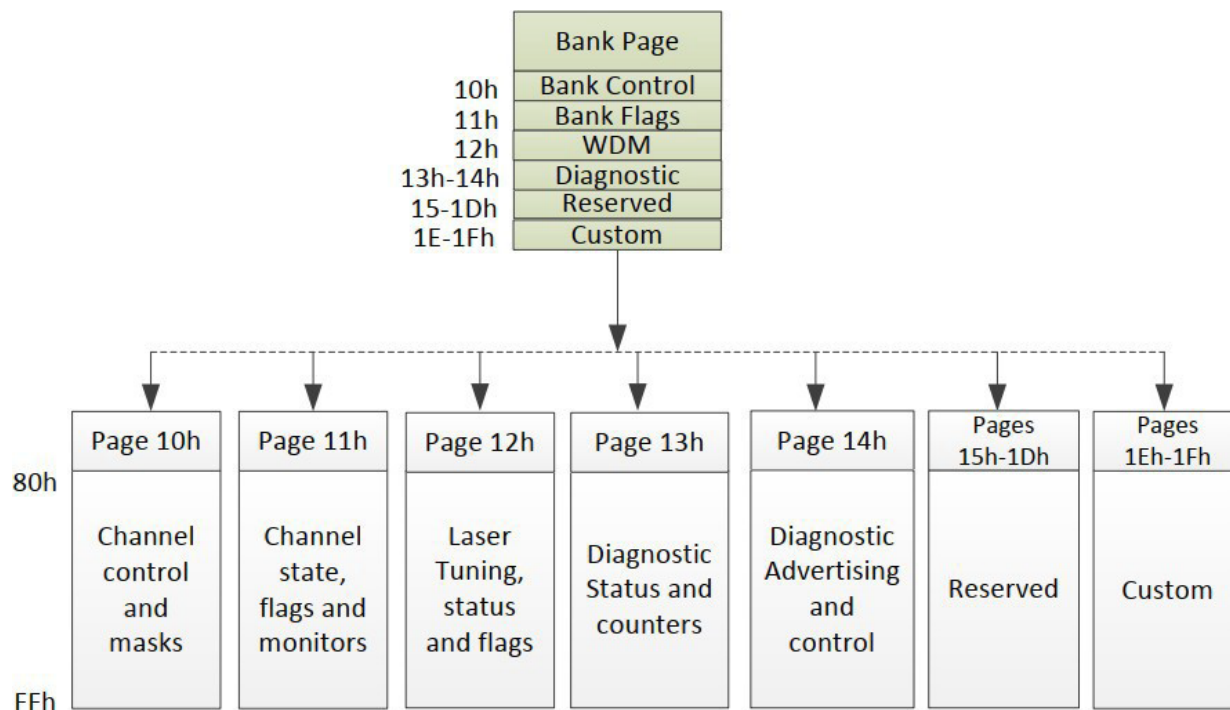


Figure 12: QSFP-DD CMIS Module Bank Page Memory Map