QDD-400G-ER4

400GBASE-ER4 QSFP-DD PAM4 LWDM4 1310nm 40km SMF LC

Features

- Supports 400GBASE-ER4;
- Lane bit rate 106.25 Gb/s with PAM4;
- Up to 40km transmission on SMF;
- Narrow LANWDM laser and PIN receiver;
- 8x53.125Gb/s with PAM4 electrical interface (400GAUI-8);
- I2C interface with integrated Digital Diagnostic monitoring;
- QSFP-DD MSA package with duplex LC connector;
- Single +3.3V power supply;
- Maximum power consumption 13W;
- Operating case temperature: 0 to +70 ° C;
- Compliant to QSFP-DD CMIS standard;
- Compliant to 802.3bs& QSFP-DD Hardware Specification;
- Complies with EU Directive 2015/863/EU;

Applications

- 400GBASE-ER4;
- 400G Ethernet;
- Data center / Cloud application.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typical	Max	Units	Notes
Storage Temperature	T_S	-40	-	+85	°C	
Supply Voltage	V_{CC}	-0.5	-	+3.6	V	
Operating Relative Humidity	RH	5	-	+85	%	

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Units	Notes
Operating Case Temperature	T_C	0	-	+70	°C	
Power Supply Voltage	V_{CC}	3.13	3.3	3.47	V	
Maximum Power Dissipation	P_D	-	-	13	W	
Aggregate Bit Rate	BR_{AVE}	-	425	-	Gb/s	With PAM4
Lane Bit Rate	BR_{LANE}	-	106.25	-	Gb/s	With PAM4
Transmission Distance	TD	-	-	40	km	Over SMF

Optical Characteristics

Transmitter						
Parameter	**Test Point**	**Min**	**Typical**	**Max**	**Units**	**Notes**
Center Wavelength Lane 0	λ0	1304.06	1304.58	1305.1	nm	
Center Wavelength Lane 1	λ1	1306.33	1306.85	1307.38	nm	
Center Wavelength Lane 2	λ2	1308.61	1309.14	1309.66	nm	
Center Wavelength Lane 3	λ3	1310.9	1311.43	1311.96	nm	
Average Launch Power per Lane	P_{TX_LANE}	1.5	-	7.1	dBm	1
OMA_{outer} per Lane	OMA_{outer}	4.5	-	7.9	dBm	2
Transmitter and dispersion eye closure for PAM4 (TDECQ), per lane	TDECQ	-	-	3.9	dB	
Average Output Power (Laser Turn off)	$P_{OUT-OFF}$	-	-	-30	dBm	
Side Mode Suppression Ratio	SMSR	30	-	-	dB	
Extinction Ratio	ER	6	-	-	dB	
Receiver						
Parameter	**Test Point**	**Min**	**Typical**	**Max**	**Units**	**Notes**
Center Wavelength Lane 0	λ0	1304.06	1304.58	1305.1	nm	
Center Wavelength Lane 1	λ1	1306.33	1306.85	1307.38	nm	
Center Wavelength Lane 2	λ2	1308.61	1309.14	1309.66	nm	
Center Wavelength Lane 3	λ3	1310.9	1311.43	1311.96	nm	
Damage threshold, per lane	P_{damage}	-2.4	-	-		3
Average Rx Power per Lane	P_{Rx} _LANE	-16.2	-	-3.4	dBm	4
Receiver sensitivity (OMA_{outer}), per lane	Sens $_{OMA}$	-	-	-14	dBm	5

Notes:

1. The optical power is launched into SMF.
2. Even if the TDECQ<1.4dB for an extinction ratio of >=4.5dB or TDECQ<1.3dB for an extinction ration of <4.5dB, the OMAouter (min) must exceed this value.
3. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level. The receiver does not have to operate correctly at this input power.
4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
5. Receiver sensitivity (OMAouter),each lane (max) is defined with BER=2.4E-4.

Electrical Characteristics

High-Speed Signal: **Compliant to 400GAUI-8 (IEEE 802.3bs) Compliant to**

Low-Speed Signal: **QSFP-DD Hardware Specification**

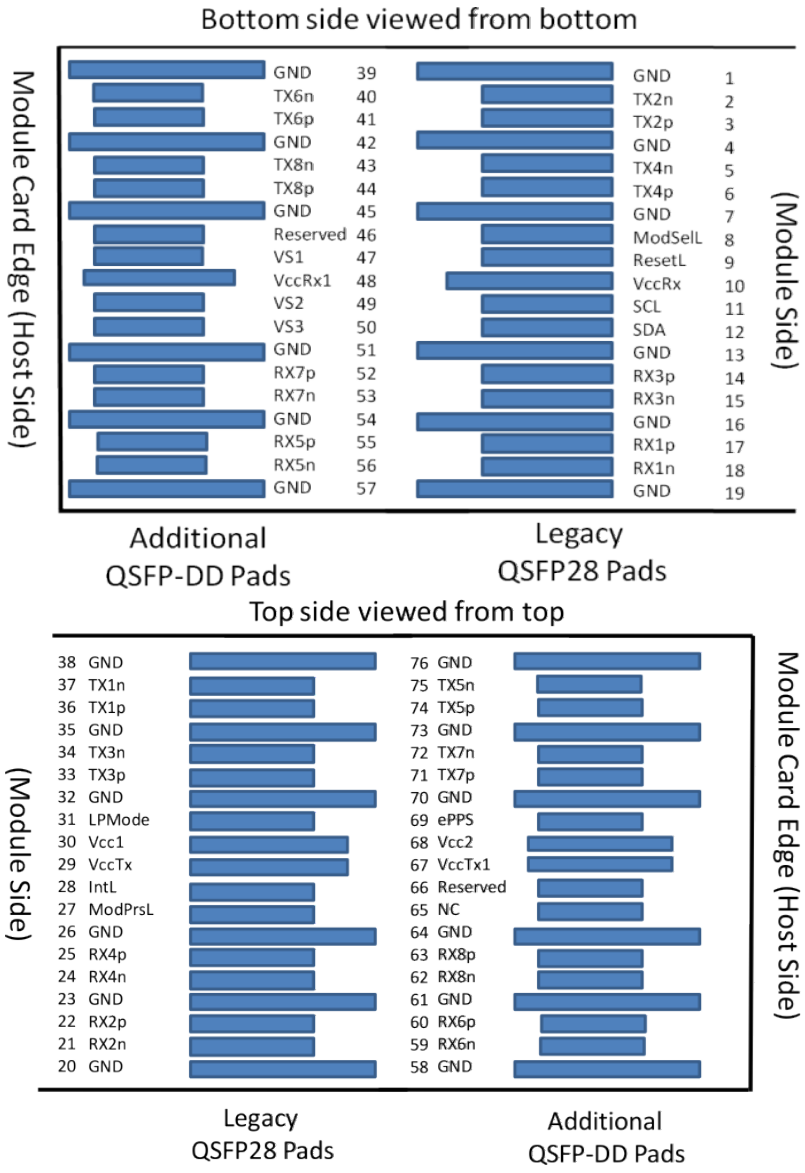
Transmitter (Module Input)						
Parameter	**Test Point**	**Min**	**Typical**	**Max**	**Units**	**Notes**
Differential Data Input Amplitude	$V_{IN,P-P}$	900	-	-	mVpp	
Differential Termination Mismatch		-	-	10	%	
Receiver (Module Output)						
Parameter	**Test Point**	**Min**	**Typical**	**Max**	**Units**	**Notes**
Differential Data Output Amplitude	$V_{OUT,P-P}$	-	-	900	mVpp	
Differential Termination Mismatch（1MHZ）		-	-	10	%	
Low-speed Electrical Interface						
LPMode/TxDis, ResetL, ModSelL and ePPS/Clock	V_{IL}	-0.3	-	0.8	V	
	V_{IH}	2.0	-	V_{CC}+0.3	V	
ModPrsL	V_{OL}	0	-	0.4	V	
	V_{IH}	ModPrsL can be implemented as a short-circuit to GND on the module				
IntL/RxLOS	V_{OL}	0	-	0.4	V	
	V_{OH}	V_{CC}-0.5	-	V_{CC}+0.3	V	

Digital Diagnostics

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 70	±3	ºC	Internal
Voltage	0 to VCC	±3%	V	Internal

Tx Bias Current per lane	0 to 100	±10%	mA	Internal
Tx Output Power per lane	1.5 to 7.1	±3	dB	Internal
Rx Power per lane	-16.2 to -3.4	±3	dB	Internal

Pin Description



Pin #	Logic	Symbol	Description	Plug Seq.	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	3B	
7		GND	Ground	1B	1
8	LVTLL-I	ModSelL	Module Select	3B	
9	LVTLL-I	ResetL	Module Reset	3B	
10		VccRx	+ 3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	3B	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	3B	
13		GND	Ground	1B	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL/RX_LOS	Interrupt/Rx LOS	3B	
29		VccTx	+3.3 V Power Supply transmitter	2B	2

30		Vcc1	+3.3 V Power Supply	2B	2
31	LVTTL-I	LPMode/Tx_DI S	Low Power mode/Tx Disable	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	

61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69		Reserved	For future use	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

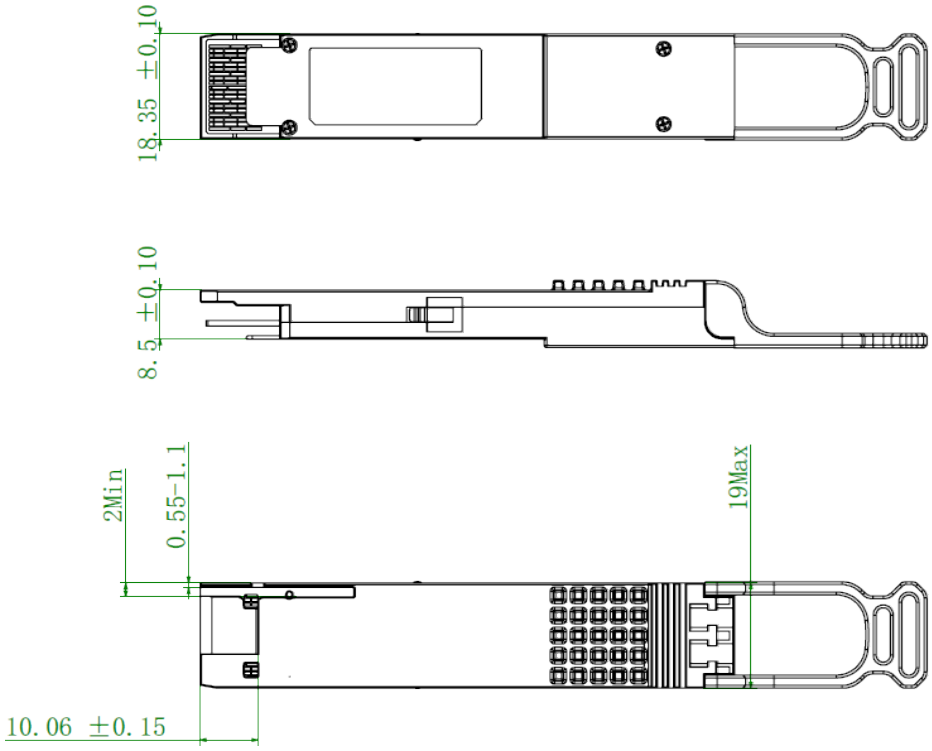
Note 1: QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP- DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

Note 3: All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A,3B.

Mechanical Dimensions



Warnings

Handling Precautions: This device is susceptible to damage as a result of electrostatic discharge (ESD). A static free environment is highly recommended. Follow guidelines according to proper ESD procedures.

Laser Safety: This Transceiver uses a semiconductor laser system and is a laser class1 product acc. FDA, complies with 21CFR1040. 10 and 1040.11. Also this product is a laser class 1 product acc. IEC 60825-1..