QDD-400G-SR4

400G QSFP-DD SR4 MMF 850nm MTP/MPO-12 60m

Features

- QSFP-DD Serial Optical Interface
  8x50G PAM4 retimed 400GAUI-8 electrical interface
  MPO-12 APC connector
  4 channel VCSEL arrays and 4 channels PIN photo detector arrays
  Maximum link length of 60m on OM3 or 100m on OM4
- QSFP-DD MSA Compliant
  Compliant to QSFP-DD Module Specification Rev 6.0
  Compliant with CMIS 5.2
- Support Protocol
  Compliant with IEEE 802.3db
  Compliant to IEEE 802.3bs
- Low Power Consumption
  Less than 9W in temperature range of 0 to 70℃
- Case temperature range: 0℃ to 70℃ (commercial)

Applications

- Data Center

1. General Description

Fibrenet' QDD-400G-SR4 is an four-Channel, Parallel, Pluggable, Fiber-Optic QSFP-DD Module for 400Gigabit Ethernet applications. This product converts 8 channels of 26.5625GBd electrical input data to 4 channels of 53.125GBd parallel optical signals. Reversely, on the receiver side, 4 channels of parallel optical signals of 53.125GBd converts to 8 channels of 26.5625GBd electrical output data. This module is designed to operate

over multimode fiber systems using a nominal wavelength of 850nm, up to 60 meters over OM3 MMF or 100 meters over OM4 MMF.

Functional Block Diagram

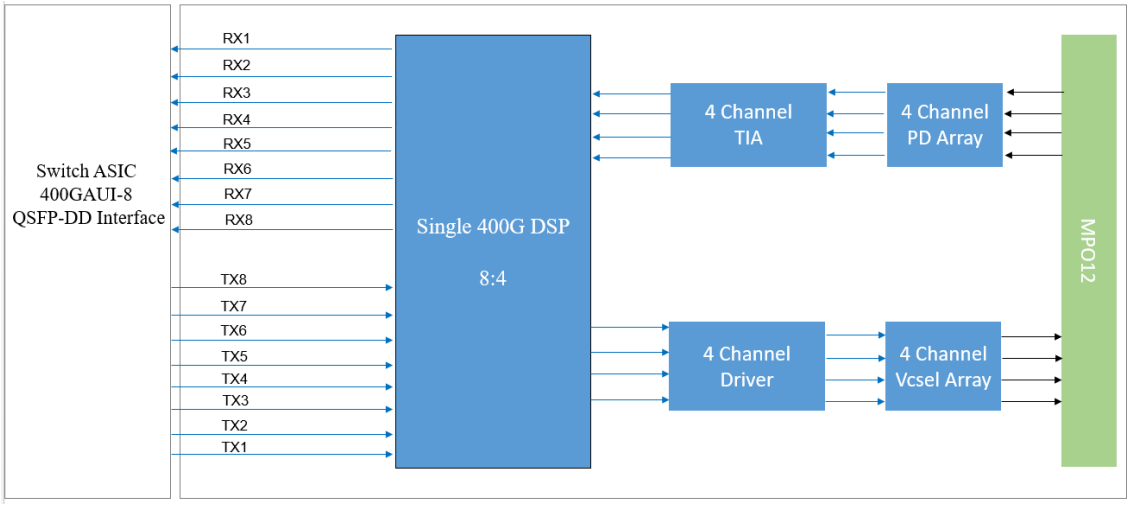


Figure 1 Functional Block Diagram

2. Absolute Maximum Ratings

Table 1 - Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature	TS	-40	85	℃
Case Operating Temperature	Top	0	70	℃
Relative Humidity (non-condensation)	RH	15	85	%
Supply Voltage	Vcc	-0.5	3.6	V
Receiver Damage Threshold, per Lane	PRdmg	5		dBm

Recommended Operating Conditions

Table 2- Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Operating Case Temperature	TC	0	70	℃
Relative Humidity(non-condensing)	RH	15	85	%
Power Supply Voltage	VCC	3.135	3.465	V
Total Power Consumption	Pc		9	W
Supply Current			2.72	A
Bit Rate	BR		425	Gbps
Fiber Length on OM3 MMF			60	m
Fiber Length on OM4 MMF			100	m
I2C Clock Frequency	0	10	1000	kHz

Notes:

1. Under condition of 3.465V operating supply voltage, and 70℃ case temperature.

3. Optical Specification

1. Optical Transmitter

Table 3- Transmitter Optical Interface

Parameter		Symbol	Min.	Typical	Max	Unit
Data rate per lane		DR		53.125		GBd
Modulation format				PAM4		
Center Wavelength 1		λ	844	850	863	nm
RMS spectral width		σ			0.6	nm
Average Launch power, each lane		Pavg	-4.6		4	dBm
Optical Power OMA, each Lane， max		POMA		3.5		dBm
OMAouter, each lane mine	max (TECQ, TDECQ) <1.8 dB			max [-2.6 , max(TECQ,TECQ) – 4.4]		dBm
	1.8 < max (TECQ, TDECQ) < 4.4 dB					
Transmitter and dispersion eye closure (TDECQ), each lane		TDECQ			4.4	dB
Transmitter eye closure for PAM4 (TECQ), each lane		TECQ			4.4	dB
Extinction ratio		ER	2.5			dB
Transmitter power excursion, each lane					2.3	dBm
Optical Return Loss Tolerance		ORLT			14	dB
Optical Power for TX DISABLE					-30	dBm
Encircled fluxb2				8.5≥86% at 19 um ≤30% at 4.5 um		

Notes:

1. Defined according to the performance of the laser used.
2. Measured into type A1a.2 or type A1a.3, or A1a.4, 50 um fiber, in accordance with IEC 61280-1-4

3.2 Optical Receiver

Table 4- Receiver Optical Interface

Parameter		Symbol	Min.	Typical	Max	Unit
Data rate per lane		BR		53.125		Gbd
Modulation format			PAM4			
Center Wavelength		λ	844	850	863	nm
Damage threshold			5			dBm
Average receive power, each lane			–6.4		4	dBm
Receive power, each lane (OMAouter)					3.5	dBm
Receiver reflectance		Rr			–15	dB
Receiver sensitivity(OMA), each lane1			RS = max (-4.6 , TECQ – 6.4)			dBm
Stressed receiver sensitivity, each lane					–2	dBm
Rx LOS	Assert		-15			dBm
	De-assert				-7.5	dBm
	Hysteresis		0.5		5	dB

Notes:

1. Receiver sensitivity is informative and is defined for a transmitter with a value of TECQ. Measured with conformance test signal at TP3 for BER = 2.4E-4 Pre-FEC.

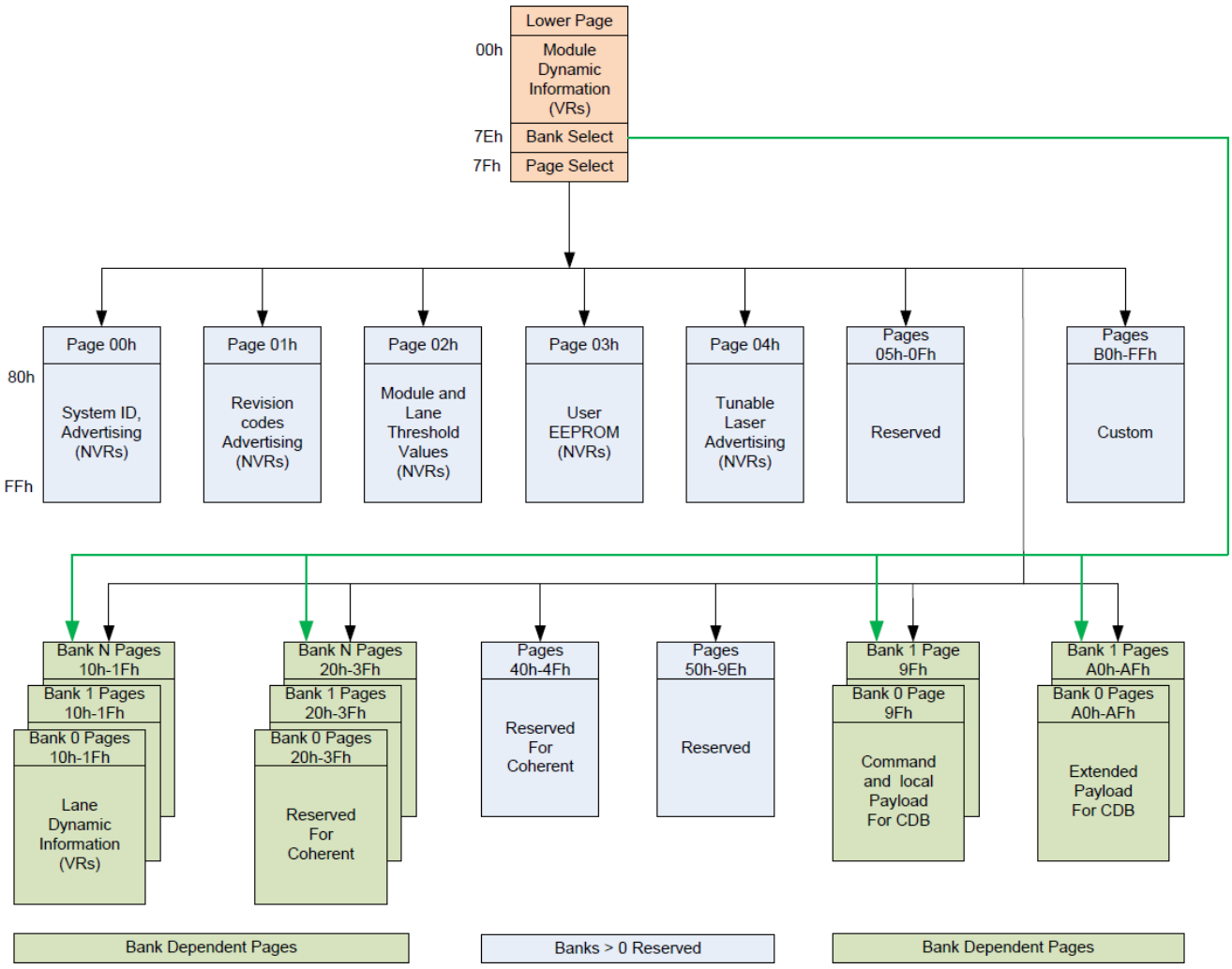
4.Electrical Specification

Table 5.1-Electrical Specifications

Parameter	Min.	Typical	Max	Unit
Supply Voltage	3.135		3.465	V
Input Differential Impedance	90	100	110	Ω
Differential data input swing			880	mVpp
Differential data output swing			900	mVpp
Bit Error Rate			2.4E-4	
Input Logic Level High	2		vcc	v
Input Logic Level High	2		vcc	v
Input Logic Level Low	0		0.8	v
Output Logic Level High	Vcc-0.5		vcc	v
Output Logic Level Low	0		0.4	v

5. User Interface

1. Management Interface



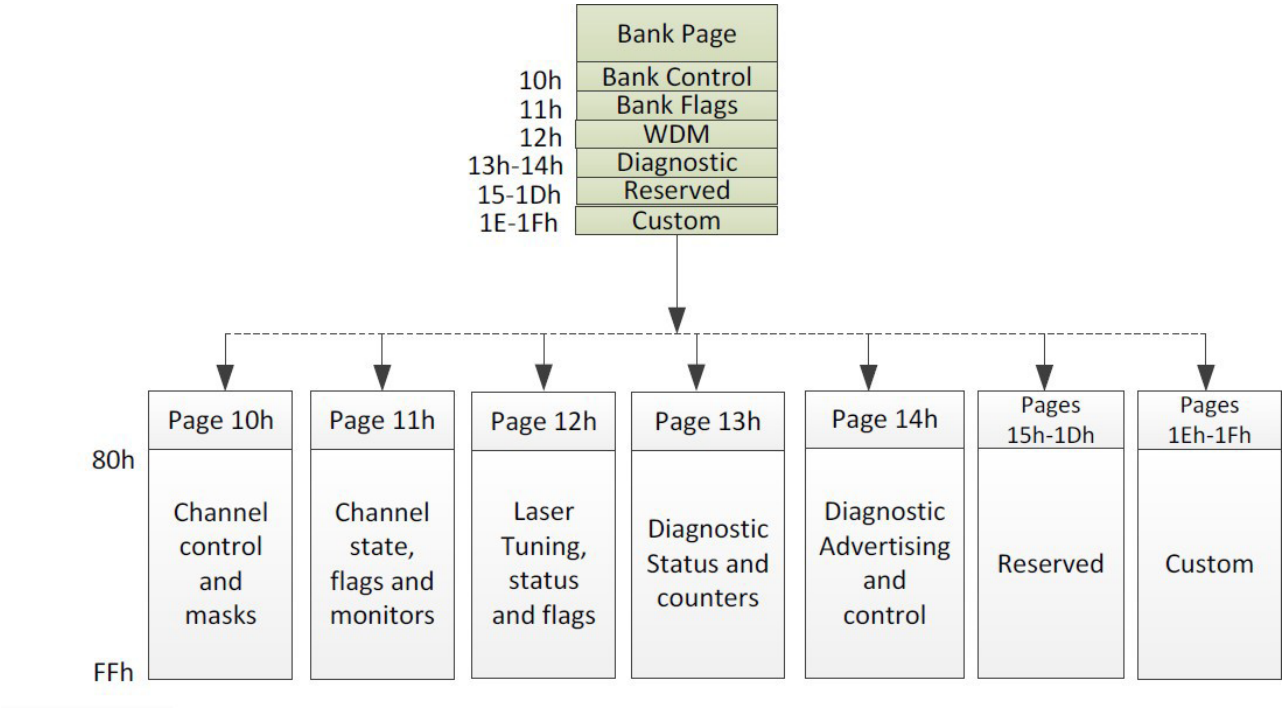


Figure 5.1 CMIS Module Memory Map

2. Multiple Applications Support

The QDD-400G-SR4 supports CMIS 5.2 defined Application Advertising, Application Selection and Instantiation.

1. Application Advertising

Table 5.2-Application Advertising

Address (Dec)	Application		Value (Hex)	Description
	AppSel Code	Name		
85	NA	Module Type encoding	1	Optical Interfaces: MMF
86	0001b	Host Interface ID	31	Host Interface ID App1: IB HDR
87		Media Interface ID	11	Media Interface ID App1: 400G-SR4
88		Host Lane Count&Media Lane Count	84	Lane Count App1: host 8 lanes, media 4 lanes
89		Host Lane Assignment Options	1	Permissible first host lane number: lane 1

01h:176		Media Lane Assignment Options	1	Permissible first media lane number: lane 1
90	0010b	Host Interface ID	11	Host Interface ID App2:400GAUI-8 C2M
91		Media Interface ID	11	Media Interface ID App2: 400G-SR4
92		Host Lane Count&Media Lane Count	84	Lane Count App2: host 8 lanes, media 4 lanes
93		Host Lane Assignment Options	1	Permissible first host lane number: lane 1
01h:177		Media Lane Assignment Options	1	Permissible first media lane number: lane 1
94	0011b	Host Interface ID	F	Host Interface ID App3:200GAUI-4
95		Media Interface ID	1B	Media Interface ID App3:200GBASE-SR2
96		Host Lane Count&Media Lane Count	42	LaneCountApp3:host 4 lanes, media 2 lanes
97		Host Lane Assignment Options	11	Permissible first host lane number: lane 1，5
01h:178		Media Lane Assignment Options	5	Permissible first media lane number: lane 1,3
98	0100b	Host Interface ID	D	HostInterfaceIDApp4: 100GAUI-2 C2M
99		Media Interface ID	D	Media Interface ID App4:100GBASE-SR1
100		Host Lane Count&Media Lane Count	21	Lane Count App4：host 2 lanes, media 1 lanes
101		Host Lane Assignment Options	55	Permissible first host lane number: lanes 1, 3，5，7
01h:179		Media Lane Assignment Options	F	Permissible first media lane number: lanes 1, 2, 3, 4
102	0101b	Host Interface ID	FF	Host Interface ID App5
103		Media Interface ID	0	Media Interface ID App5
104		Host Lane Count&Media Lane Count	0	Lane Count App5
105		Host Lane Assignment Options	0	Host Lane Assignment Options App5

As shown in the table above, the QDD-400G-SR4 supports 4 applications, IB HDR 400GBASE-SR4 and Ethernet 400GBASE-SR4,200GBASE-SR2,100GBASE-SR1.

5.2.2 Application Selection and Instantiation

The host can select Applications by programming the AppSel value in Staged Set 0. AppSel=1 is the default Application populated in the Active Control Set at power-on or reset.

* Note that the channels of the module are independent and can be configured separately.(ie. up to four 100GBASE-SR instances can be configured), however, it does not support different applications with different channels at the same time.

QDD-400G-SR4 supports two methods of application selection and instantiation. The first method is implemented according to CMIS, and the second method is customized, which is simpler.

1. First mothod:

The applications switching configuration sequence is as follows: read Application Descriptor Registers and select the required Appsel. Write application configuration to DPConfigLane<i> in Stage Control Set 0, then write 1 to ApplyDPInitLane<i> to trigger Application Instantiation. The Active Set can be read from page11h.

For example, select AppDescriptor3:

Step 1: Write 0x30 in Page10h Byte145~Byte152(8 bytes)—Set AppselCode3

Step 2: Write 0xFF in Page10h Byte143—Set trigger register to run Application Instantiation.

2. Second mothod:

Set the value of Page10h Byte240. This is a private definition.

Table 5.3 Private Host Electrical Interface Codes

Code Value	Bit Pattern	Host Electrical Interface	Media Interface
0	00000000b	IB HDR	400GBASE-SR4
1	00000001b	400GAUI-8 C2M	400GBASE-SR4
2	00000010b	200GAUI-4 C2M	200GBASE-SR2
3	00000011b	100GAUI-2 C2M	100GBASE-SR

3. TX & RX Squelch

Default TX and RX auto-squelch is enabled. But TX and RX auto squelch disable, and force squelching function are not supported.

4. TX input equalization

Default TX adaptive equalization is enabled. But TX adaptive equalization disable, and fixed equalization adjust function are not supported.

5. RX output Equalization

RX output Equalization follows CMIS Table 6-7, with default 1dB, readable and writable.

Table 6-7 Rx Output Equalization Codes

Code Value	Bit pattern	Post-Cursor Equalization	Pre-Cursor Equalization
0	0000b	0dB (No Equalization)	0dB (No Equalization)
1	0001b	1 dB	0.5 dB
2	0010b	2 dB	1.0 dB
3	0011b	3 dB	1.5 dB
4	0100b	4 dB	2.0 dB
5	0101b	5 dB	2.5 dB
6	0110b	6 dB	3.0 dB
7	0111b	7 dB	3.5 dB
8-10	1000b-1010b	Reserved	Reserved
11-15	1011b-1111b	Custom	Custom

Table 5.4 QSFP-DD Rx Output Equalization code table

5.6 RX output amplitude

RX output amplitude follows CMIS Table 6-8, Rx output amplitude is the difference peak-to- peak EYE high when Rx output equalization is set to 0dB. The default value of output amplitude is set to 2, with typical differential 600mVp-p.

Table 6-7 Rx Output Amplitude Codes

Code Value	Bit pattern	Output Amplitude
0	0000b	100-400 mV (P-P)
1	0001b	300-600
2	0010b	400-800
3	0011b	600-1200
4-14	0100b-1110b	Reserved
15	1111b	Custom

Table 5.6 QSFP-DD Rx Output Amplitude code table

5.7 Loopback capabilities

Media side input loopback and Host side input loopback feature are supported, loopback control method refers to CMIS.

Table 5.7 QSFP-DD Rx Output Equalization code table

Byte	Bites	Field Name	Field Description
13h:128	6	Simultaneous Host And Media Side loopbacks	0b: not supported
	5	Per Lane Media Side Loopbacks	1b: supported
	4	Per Lane Host Side Loopbacks	1b: supported
	3	Host Side Input Loopback	1b: supported
	2	Host Side Output Loopback	1b: supported
	1	Media Side Input Loopback	1b: supported
	0	Media Side Output Loopback	1b: supported

5.8 Digital Diagnostic Monitor Accuracy

The following characteristics are defined over recommended operating conditions.

Table 5.4 Digital Diagnostic Monitor Accuracy

Parameter	Accuracy	Unit
Internally measured transceiver temperature1	+/-3	℃
Internally measured transceiver supply voltage	+/-3	%
Measured Tx bias current	+/-10	%
Measured Tx output power2	+/-3	dB
Measured Rx received average optical power	+/-3	dB

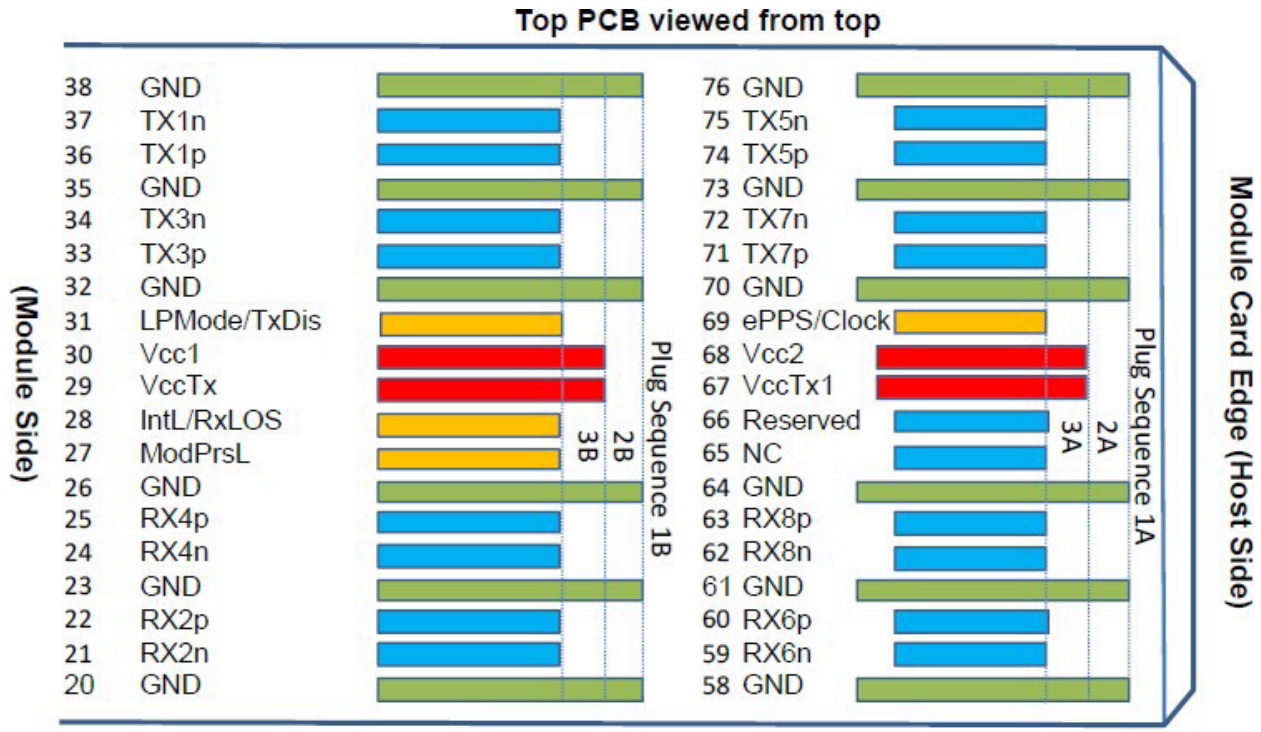
Notes:

1. Test point is the hotspot of the module.
2. DDM reports stability within 0.5 dB when temperature is stable. TX DDM reportes -40 dBm when TX disable.

6. Pin Assignment and Description

1. PIN Definitions

QSFP-DD Transceiver Pad Layout, host PCB QSFP-DD Pinout, and PIN Descriptions are as follows:



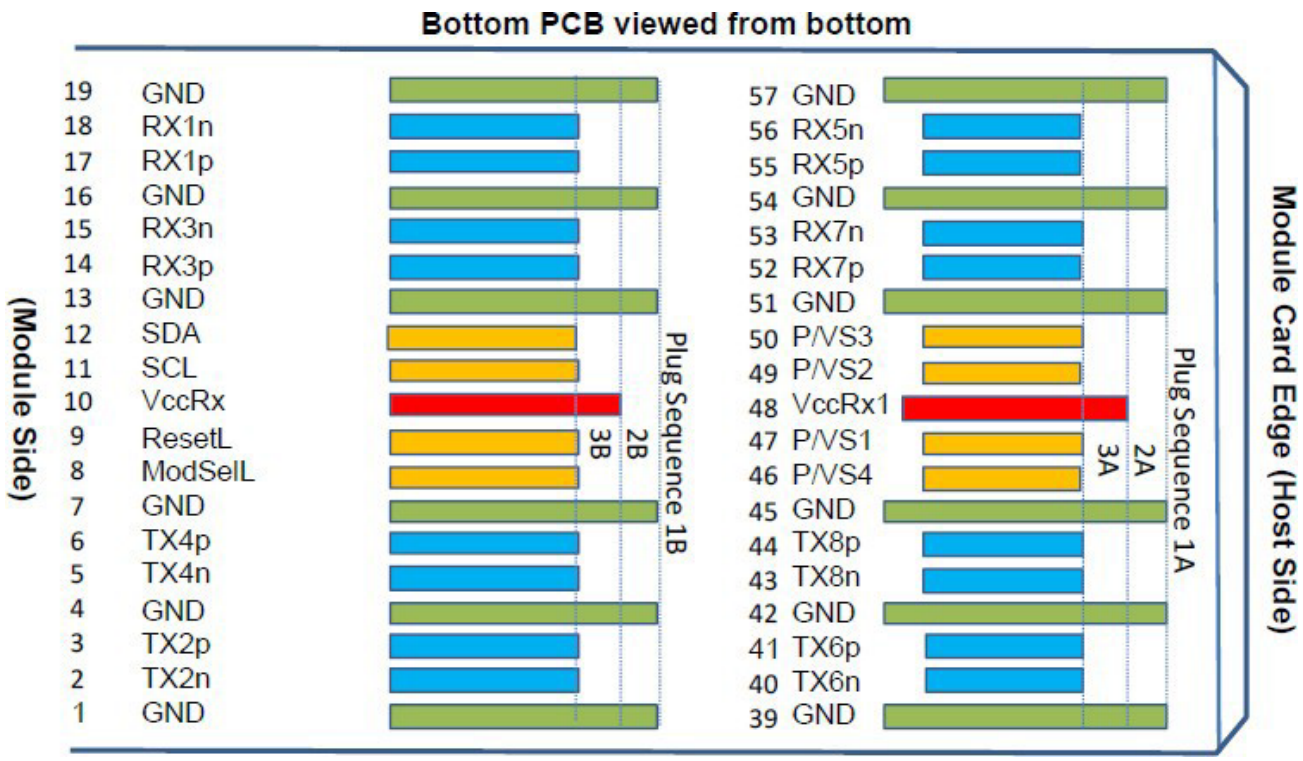


Figure 6.1 QSFP-DD Transceiver Electrical Pad Layout

6.2 Pin Description

Table 6.2- Pin Description

PIN	Name	Logic	Description	Plug Sequence	Notes
1	Ground		GND	1B	1
2	Tx2n	CML-I	Transmitter Inverted Data Input	3B	
3	Tx2p	CML-I	Transmitter Non-Inverted Data Input	3B	
4	Ground		GND	1B	1
5	Tx4n	CML-I	Transmitter Inverted Data Input	3B	
6	Tx4p	CML-I	Transmitter Non-Inverted Data Input	3B	
7	Ground		GND	1B	1
8	ModSelL	LVTTL-I	Module Select	3B	

9	ResetL	LVTTL-I	Module Reset	3B	
10	VccRx		+3.3V Power Supply Receiver	2B	2
11	SCL	LVCMOSI/O	2-wire serial interface clock	3B	
12	SDA	LVCMOSI/O	2-wire serial interface data	3B	
13	Ground		GND	1B	1
14	Rx3p	CML-O	Receiver Non-Inverted Data Output	3B	
15	Rx3n	CML-O	Receiver Inverted Data Output	3B	
16	Ground		GND	1B	1
17	Rx1p	CML-O	Receiver Non-Inverted Data Output	3B	
18	Rx1n	CML-O	Receiver Inverted Data Output	3B	
19	Ground		GND	1B	1
20	Ground		GND	1B	1
21	Rx2p	CML-O	Receiver Non-Inverted Data Output	3B	
22	Rx2n	CML-O	Receiver Inverted Data Output	3B	
23	Ground		GND	1B	1
24	Rx4p	CML-O	Receiver Non-Inverted Data Output	3B	
25	Rx4n	CML-O	Receiver Inverted Data Output	3B	
26	Ground		GND	1B	1
27	ModPrsl	LVTTL-O	Module Present	3B	
28	IntL	LVTTL-O	Interrupt	3B	
29	VccTx		+3.3V Power supply transmitter	2B	2
30	Vcc1		+3.3V Power supply	2B	2
31	LPMode	LVTTL-I	Low Power mode	3B	
32	Ground		GND	1B	1

33	Tx3p	CML-I	Transmitter Non-Inverted Data Input	3B	
34	Tx3n	CML-I	Transmitter Inverted Data Input	3B	
35	Ground		GND	1B	1
36	Tx1p	CML-I	Transmitter Non-Inverted Data Input	3B	
37	Tx1n	CML-I	Transmitter Inverted Data Input	3B	
38	Ground		GND	1B	1
39	Ground		GND	1A	1
40	Tx6n	CML-I	Transmitter Inverted Data Input	3A	
41	Tx6p	CML-I	Transmitter Non-Inverted Data Output	3A	
42	Ground		GND	1A	1
43	Tx8n	CML-I	Transmitter Inverted Data Input	3A	
44	Tx8p	CML-I	Transmitter Non-Inverted Data Output	3A	
45	Ground		GND	1A	1
46	Reserved		For future use	3A	3
47	VS1		Module Vendor Specific1	3A	3
48	VccRx1		3.3V Power Supply	2A	2
49	VS2		Module Vendor Specific2	3A	3
50	VS3		Module Vendor Specific3	3A	3
51	Ground		GND	1A	1
52	Rx7p	CML-O	Receiver Non-Inverted Data Output	3A	
53	Rx7n	CML-O	Receiver Inverted Data Output	3A	
54	Ground		GND	1A	1
55	Rx5p	CML-O	Receiver Non-Inverted Data Output	3A	
56	Rx5n	CML-O	Receiver Inverted Data Output	3A	

57	Ground		GND	1A	1
58	Ground		GND	1A	1
59	Rx6n	CML-O	Receiver Inverted Data Output	3A	
60	Rx6p	CML-O	Receiver Non-Inverted Data Output	3A	
61	Ground		GND	1A	1
62	Rx8n	CML-O	Receiver Inverted Data Output	3A	
63	Rx8p	CML-O	Receiver Non-Inverted Data Output	3A	
64	Ground		GND	1A	1
65	NC		No Connect	3A	3
66	Reseved		For future use	3A	3
67	VccTx1		3.3V Power Supply	2A	2
68	Vcc2		3.3V Power Supply	2A	2
69	ePPS	LVTTL-I	Precision Time Protocol (PTP) reference clock input	3A	3
70	Ground		GND	1A	1
71	Tx7p	CML-I	Transmitter Non-Inverted Data Output	3A	
72	Tx7n	CML-I	Transmitter Inverted Data Output	3A	
73	Ground		GND	1A	1
74	Tx5p	CML-I	Transmitter Non-Inverted Data Output	3A	
75	Tx5n	CML-I	Transmitter Inverted Data Output	3A	
76	Ground		GND	1A	1

Notes:

1. QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.

2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10Kohms and less than 100 pF.

4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A,2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.

7. Mechanical Dimensions

1. Package dimensions

Figure 7.1 shows the package dimensions of the module. Package dimensions are specified in QSFP-DD MSA.

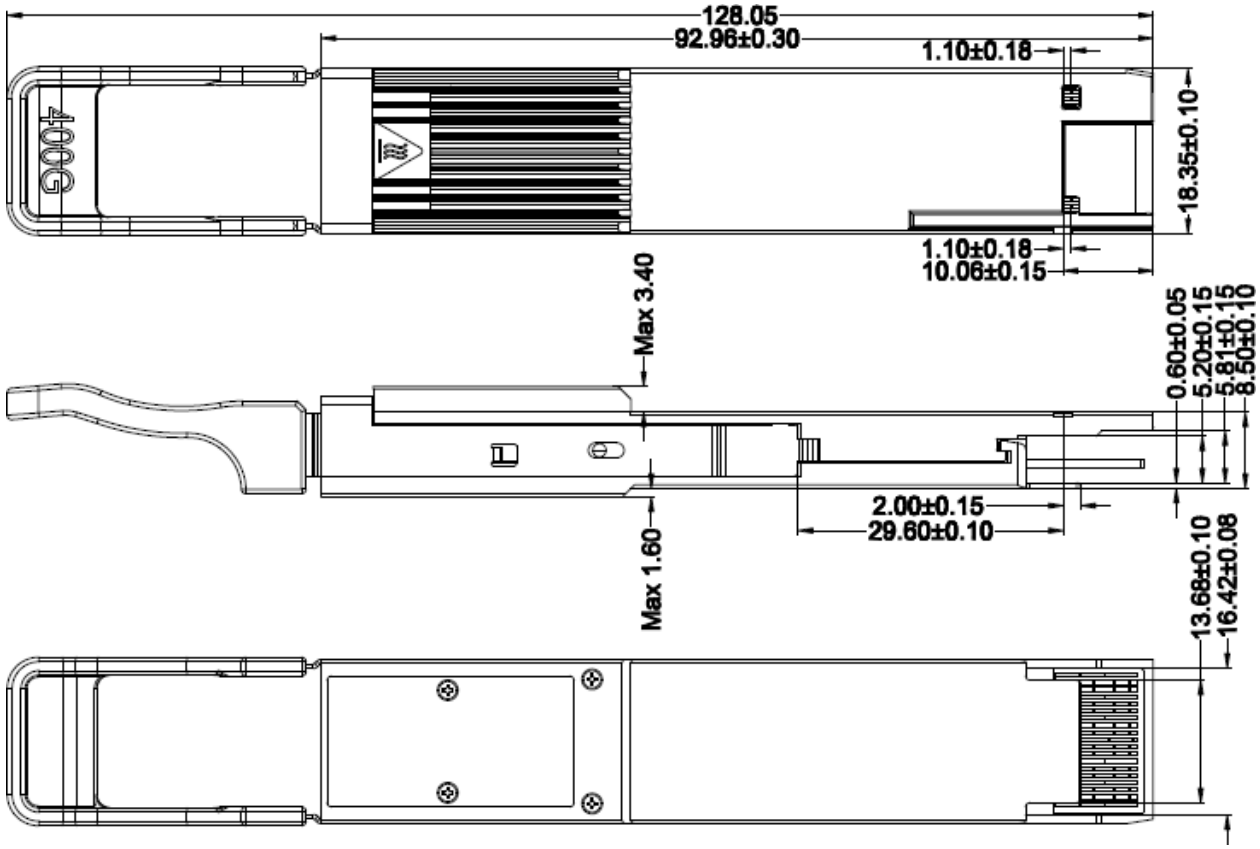


Figure 7.1 Package dimensions

7.2 Pull-tab Color

Pull-tab color is Pantone 475U (Beige).

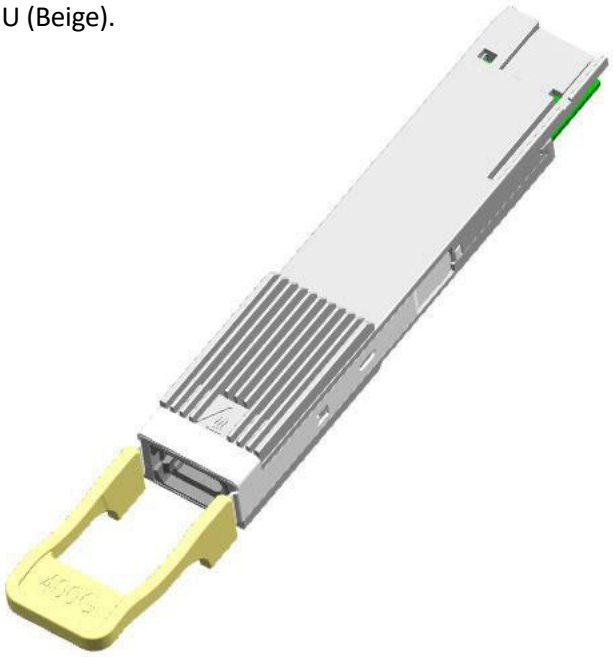


Figure 7.2 MPO12 Module appearance

7.3 Optical interface requirement

The optical port provide MPO12 APC as follow：

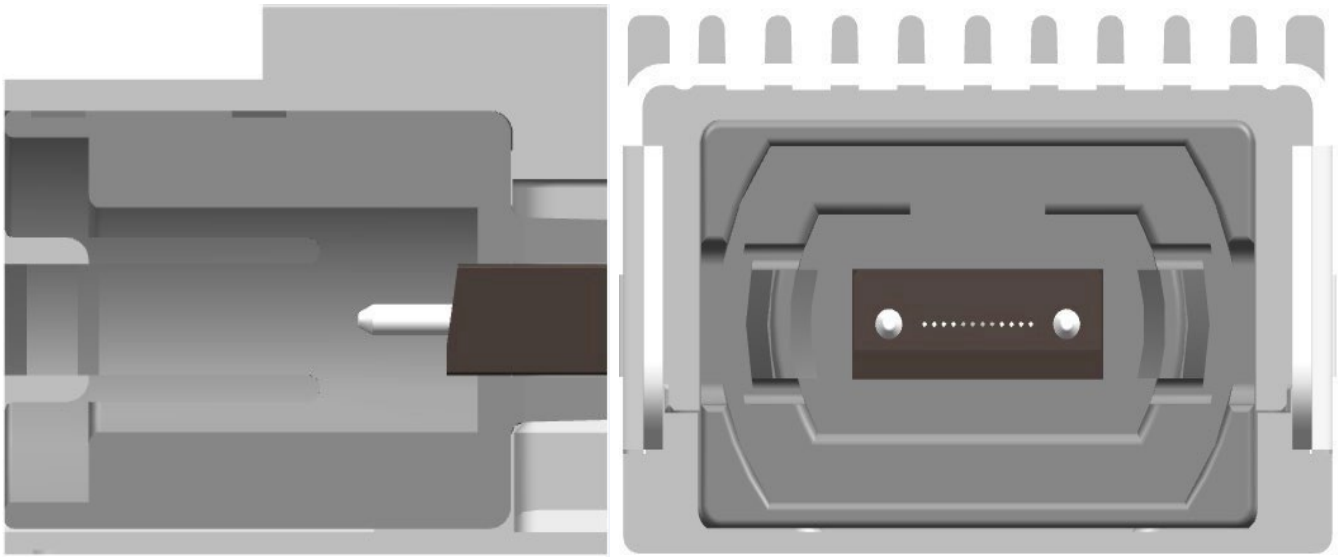


Figure 7.3 MPO12 APC connector fiber lane assignments

8. Laser safety and Electromagnetic Compatibility

1. Laser safety

The QDD-400G-SR4 are Class 1 Laser products according to FDA/CDRH、IEC-60825-1 and IEC60825-2 standards.

They must be operated under the specified operating conditions.

2. Electromagnetic Compatibility

The QDD-400G-SR4 C are designed to meet FCC Class B limits.

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