QSFP-100G-LR4-OTU

100GBASE LR4 and OTU4 QSFP28 multi-rate transceiver, DML laser, LC, SMF, 10km, DOM

- Compliant with the QSFP28 MSA Technical Specifications.
- Supports multi-rate (100GBASE 100GE and OTU4); from 103.1Gb/s to 111.8Gb/s aggregate
- Lane bit rate 25.78 Gb/s 100GE, 27.95 Gb/s OTU4;
- Maximum link length of 10km on Single Mode Fiber (SMF)
- Optical specifications are compliant with IEEE802.3ba 100GBASE-LR4.
- Low speed electrical signal is compliant with SFF-8679
- High speed electrical signal is compliant with 802.3bm CAUI-4
- Digital diagnostic functions are available via the I2C interface, as specified by SFF-8636
- 4x25Gb/s DFB-based LAN-WDM transmitter with central wavelengths of 4 channels 1295.56, 1300.05, 1304.58 and 1309.14 nm
- Supports operation for a case temperature of 0°C to +70 °C
- Duplex LC receptacles
- Power Dissipation < 4W
- Single 3.3V Power Supply
- ROHS Compliant.

Applications

- 100GBASE-LR4 Ethernet links.

Description

Fibrenet QSFP28 LR4 is a 4x25G singlemode fiber, hot pluggable optical transceiver. Unique System On Glass TM (SOGTM) technology enables the integration of 4 transmitters, 4 receivers and an optical MUX/DEMUX into a small form factor package that delivers up to 112 Gbps data link in a compact QSFP28 footprint.

The optical connectivity is based on two Single mode Fiber (SMF) LC connectors, one for Tx and one for Rx. The Tx and Rx each consist of 4 x 25GB/s LAN-WDM channels , whose wavelengths are in the 1300nm range The QSFP28 LR4 transceiver is designed for applications with a reach up to 10Km. This transceiver is based on proprietary PLC technology, using surface mounted opto-electronic devices with no free space elements. The unique design of the optical engine facilitates unparalleled compactness while maintaining Telcordia robustness.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Storage Temperature Range	TSTG	_40	+85	℃
Supply Voltage	Vcc	0	4	V
Maximum Average Input Optical Power per Lane (Damage Threshold)	PIN	5.5		dBm
Relative Humidity	RH	10% to 90% non-condensing		

Operating Conditions

Parameter	Symbol	Min	Typical	Max	Units
Case Temperature-Operating	TCASE	0		70	℃
Supply Voltage	Vcc	3.14	3.3	3.46	V
Power Consumption	PDISS			3.5	W
Aggregate Bit Rate	BR_{AVE}		103.125		Gb/s
Lane Bit Rate	BR_{LANE}		25.78	27.952	Gb/s
Power Consumption-LP Mode	PDISS-lp			1.5	W

100GBASE-LR4 Operation

Parameter	Lane	Min	Typical	Max	Unit	Notes
Signaling rate, each lane		25.78125 ± 100 ppm / 27.952 ± 100 ppm			Gb/s	
Lane Wavelength Range Lane	Lane 0	1294.53		1296.59	nm	
	Lane 1	1299.02		1301.09	nm	
	Lane 2	1303.54		1305.63	nm	
	Lane 3	1308.09		1310.09	nm	
Average Optical Power per lane		-4.3		4.5	dBm	
Total Average Launch Power				10.5	dBm	
Optical Modulation Amplitude(OMA), each lane		-1.3		4.5	dBm	
Launch Power in OMAminusTDPeachlane		-2.3			dBm	
Transmitter and Dispersion Penalty(TDP)each lane				2.2	dB	
Average Launch Power per Lane @TXOff State				-30	dBm	

Extinction Ratio		4			dB	
Relative Intensity Noise(OMA)				-130	dB/Hz	
Side-Mode Suppression Ration(SMSR)				30	dB	
Optical Return LossTolerance						

Notes:

1. The optical power is launched into SMF.
2. Measured with a PRBS 2^{31}-1 test pattern @25.78125/27.952 Gb/s, Hit ratio≤5E-5.
3. Measured with a PRBS 2^{31}-1 test pattern @25.78125 Gb/s, BER≤1E-12.
4. Measured with a PRBS 2^{31}-1 test pattern @27.952 Gb/s, BER≤1E-12(with FEC), BER≤1E-6(Pre-FEC).

Pin Description

The electrical interface to the transceiver is a 38 pins edge connector. The 38 pins provide high speed data, low speed monitoring and control signals, I2C communication, power and ground connectivity. The top and bottom views of the connector are provided below, as well as a table outlining the contact numbering, symbol and full description.

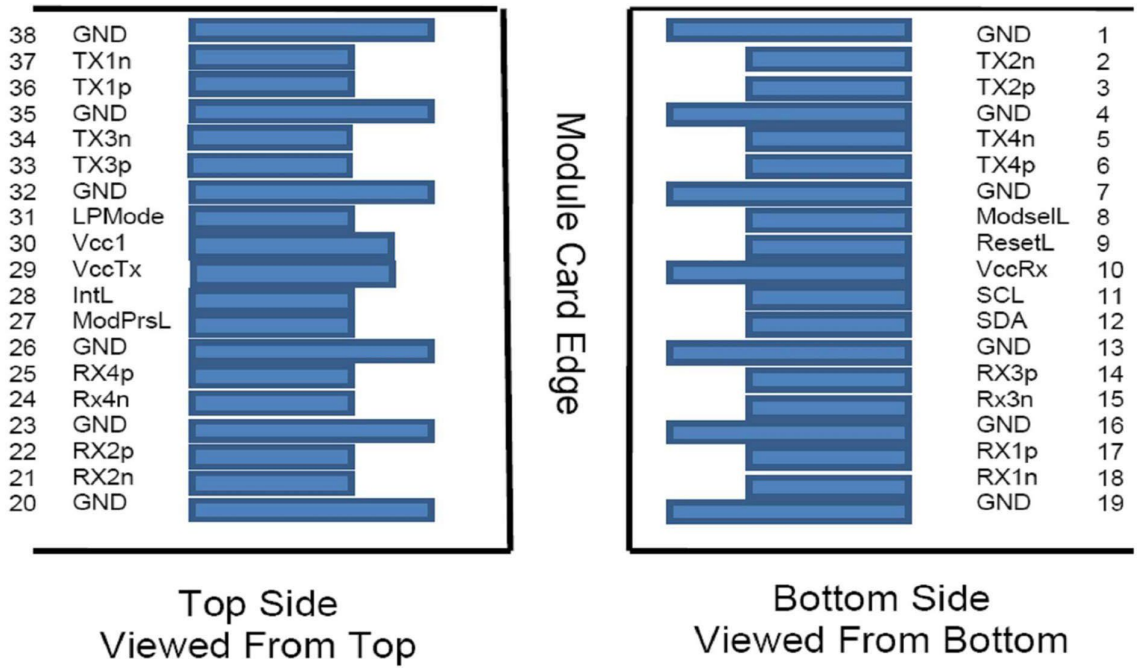

Figure 1. QSFP28-compliant 38-pin connector

Electrical Characteristics

Transmitter electrical input signal characteristics(TP1)	Min	Typical	Max	Unit
Signaling rate per lane (range)	25.78125 ± 100 ppm / 27.952 ± 100 ppm			GBd
Differential input return loss	Equation (83E–5)			dB
Differential to common mode input return loss	Equation (83E–6)			dB

Differential termination mismatch			10	%
Module stressed input test	See 83E3.4.1			
Differential pk-pk input voltage tolerance	900			mV
DC common mode voltage	-350		2850	mV
Single ended voltage tolerance range	-0.4		3.3	V
Receiver electrical output signal characteristics(TP4)	**Min**	**Typical**	**Max**	**Unit**
Signaling rate per lane (range)	25.78125 ± 100 ppm/ 27.952 ± 100 ppm			GBd
AC common-mode output voltage (RMS)			17.5	mV
Differential output voltage			900	mV
Eye width	0.57			UI
Eye height, differential	228			mV
Vertical eye closure			5.5	dB
Differential output return loss	Equation (83E–2)			dB
Common to differential mode conversion return loss	Equation (83E–3)			dB
Differential termination mismatch			10	%
Transition time (20% to 80%)	12			ps
DC common mode voltage	-350		2850	mV

Functional Block Diagram

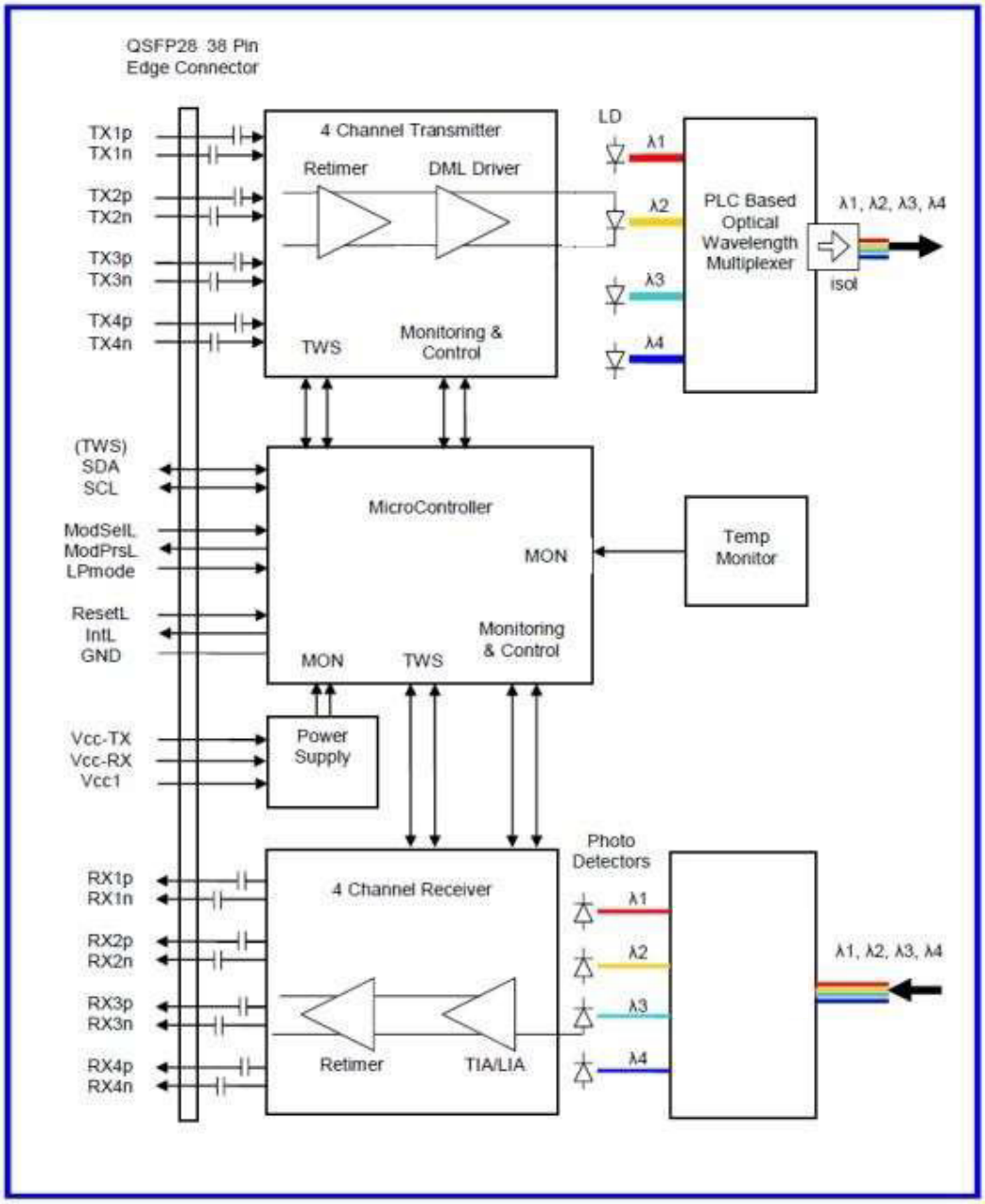

Figure 2. Functional Block Diagram

QSFP Transceiver Pinout

PIN	Logic	Symbol	Description	Plug Seq.	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	3	
7		GND	Ground	1	1
8	LVTLL-I	ModSelL	Module Select	3	
9	LVTLL-I	ResetL	Module Reset	3	
10		VccRx	+ 3.3V Power Supply Receiver	2	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	3	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	3	
13		GND	Ground	1	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL/Rx Los	Interrupt / Rx los output	3	

29		VccTx	+3.3 V Power Supply transmitter	2	2
30		Vcc1	+3.3 V Power Supply	2	2
31	LVTTL-I	LPMode/Tx dis	Low Power Mode / Tx disable input	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Output	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Output	3	
38		GND	Ground	1	1

Note 1: GND is the symbol for signal and supply (power) common for the QSFP28 module. All are common within the QSFP28 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in MSA. The connector pins are each rated for a maximum current of 1000 mA.

Mechanical Specifications

Unit: mm